

# Ares-1 (LAR-1)

## Cometlake-U Schematics

Project Code: 4PD0HK010001  
PCB(Raw Card): 18834-1M

2020-03-19

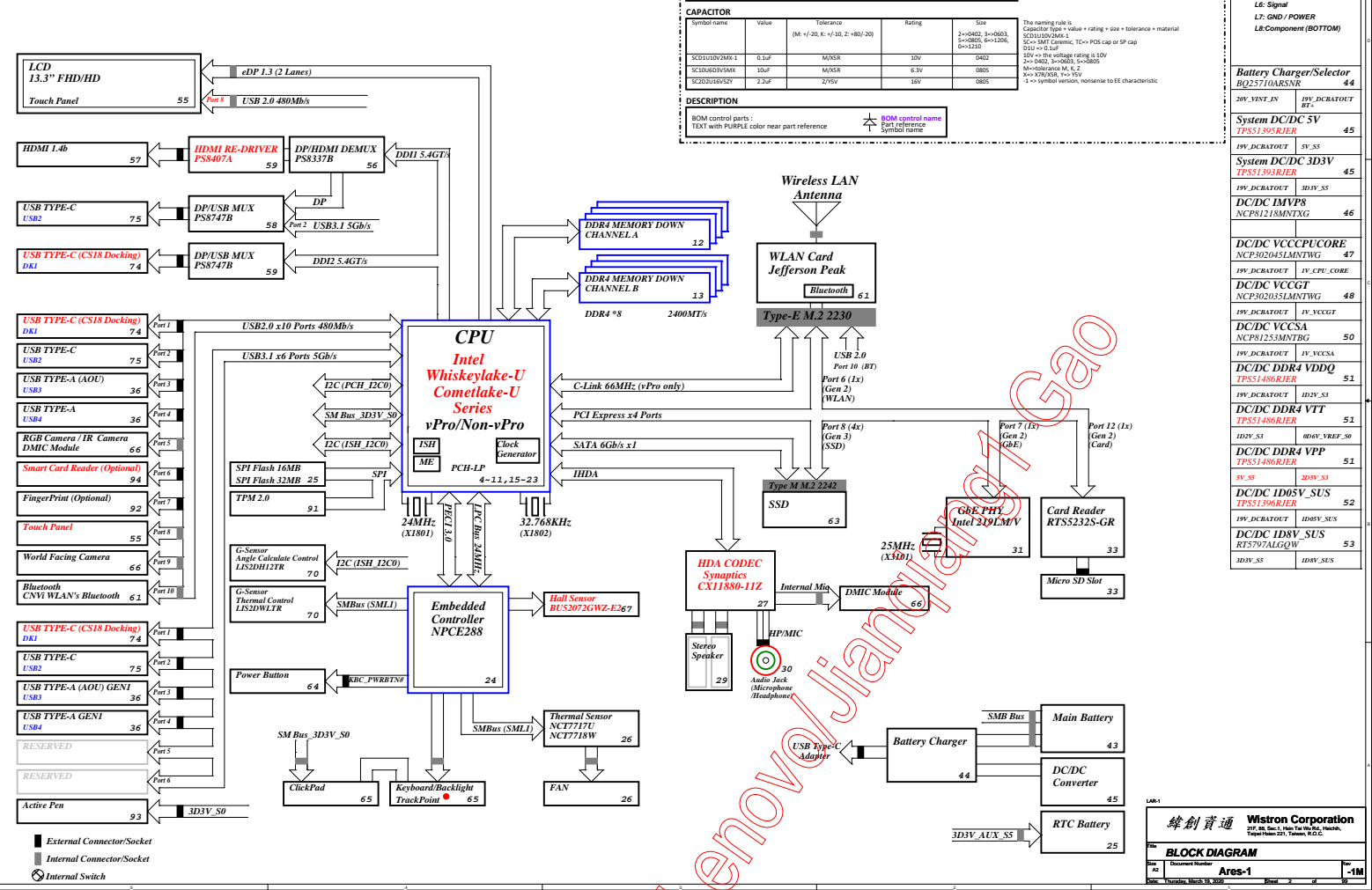
DY	DUMMY
PCBID	PCB NO. control for SW
SKUID	CPU Type change for SW
MEM_ID	Memory ID for SW
DDR4_CTRL	SDP DDP setting
SDP/DDP	Select single DIE (SDP) Dual DIE(DDP)
APS/ISH/LPC/XDP	Debug Connectors
EMC	For EMC test request
NON_PSL/PSL	KBC PSL model control
CHARGER_HS/CHARGER_LS	Charger High/Low side MOSFET
VCCSA_HS/VCCSA_LS	VCCSA High/Low Side MOSFET
YOGA	YOGA model setting
ZZ	For Test Piont /Hole /ShortPad

LAR-1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>COVER PAGE</b>			
Size A4	Document Number <b>Ares-1</b>		Rev <b>-1M</b>
Date: Thursday, March 19, 2020		Sheet 1 of 99	

# Ares-1 Cometake-U Block Diagram

Project Code: 4PD0HK010001  
PCB(Raw Card): 18834-SB



### RESISTOR

Symbol name	Value	Tolerance	Rating	Size
100K3	10K Ohm	(J: 5%, F: 1%, D: 0.5%, B: 0.1%)	0402 => 1/16W, 75V 0805 => 1/10W, 75V 0805 => 1/10W, 100V	2==0402, 3==0603, 4==0805, 5==1206, 6==1210
100K3	10K Ohm	If no letter, it means ± 5%	1/16W, 75V	0603
100K3	10K Ohm	If no letter, it means ± 5%	1/10W, 100V	0805
100K3	10K Ohm	F: 1%	1/16W, 75V	0603

### CAPACITOR

Symbol name	Value	Tolerance	Rating	Size
SC01050V2MX-1	0.1uF	NO/NA	10V	0402
SC01050V2MX	10uF	NO/NA	6.3V	0805
SC01050V2MX	2.2uF	20%	16V	0805

The naming rule is:  
Capacitor type + value + rating + size + tolerance + material  
For the value, it can be read by the number before R, (R means resistor)  
For the tolerance, it can be read from the last letter.  
For the rating, we don't show on the symbol name.  
For the size, R2==0402, R3==0603, R5==0805, ...  
10V = the voltage rating is 10V  
2==0402, 3==0603, 4==0805,  
5==1206, 6==1210, ...  
K=Keram, R=Resistor, ...  
1 == symbol version, otherwise to EE characteristic

### DESCRIPTION

BOM control parts:  
TEXT with PURPLE color near part reference

★ BOM control name  
★ Part reference  
★ Symbol name

### PCB Layer Stackup

8 Layers FR4 (8-1.0-15L)  
L1: Component (TOP)  
L2: Signal / GND / POWER  
L3: Signal / GND / POWER  
L4: Signal / GND / POWER  
L5: Signal / GND / POWER  
L6: Signal  
L7: GND / POWER  
L8: Component (BOTTOM)

### Battery Charger/Selector

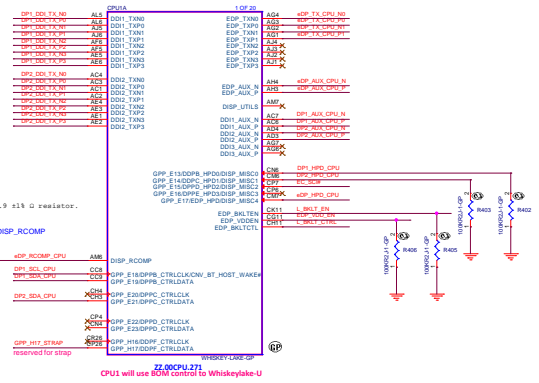
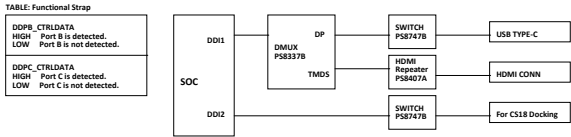
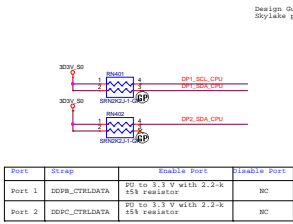
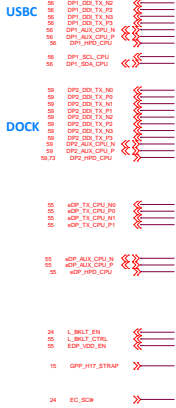
BQ25710ARSNR 44  
20V\_VENT\_IN 20V\_DCRATOUT\_BT  
System DC/DC 5V  
TPS51395RJR 45  
10V\_DCRATOUT 3V\_SS  
System DC/DC 3D3V  
TPS51395RJR 45  
10V\_DCRATOUT 3D3V\_SS  
DC/DC IMVP8  
NCP81218MNTXG 46  
DC/DC VCCCPUCORE  
NCP3020451AMTWG 47  
10V\_DCRATOUT 1V\_CPU\_CORE  
DC/DC VCCGT  
NCP3020351AMTWG 48  
10V\_DCRATOUT 1V\_VCCGT  
DC/DC VCCSA  
NCP81253MNTG 50  
10V\_DCRATOUT 1V\_VCCSA  
DC/DC DDR4 VDDQ  
TPS51466RJR 51  
10V\_DCRATOUT 1D3V\_SS  
DC/DC DDR4 VTT  
TPS51466RJR 51  
1D3V\_SS 10V\_VREF\_30  
DC/DC DDR4 VPP  
TPS51466RJR 51  
1V\_SS 30V\_VSS  
DC/DC IDB5V\_SUS  
TPS51466RJR 52  
10V\_DCRATOUT 1D3V\_SS  
DC/DC IDB8V\_SUS  
RTS5232S-GR 53  
3D3V\_SS 10V\_VSS

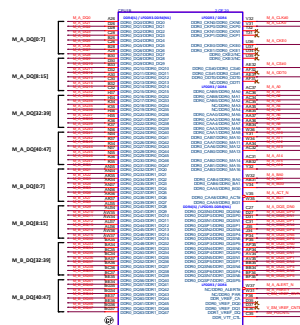
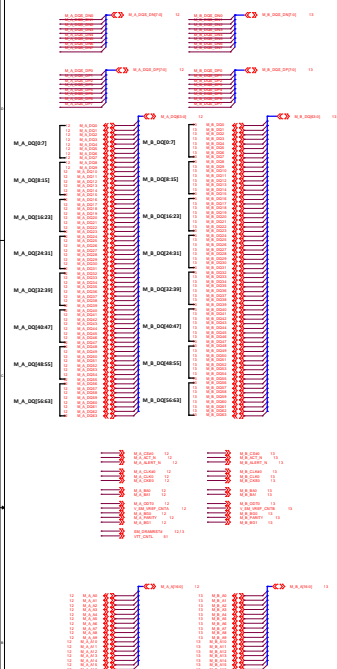
### WISTRON CORPORATION

WISTRON CORPORATION  
22F, 2nd Fl., No. 7, Heping Rd., Taipei 106, Taiwan, R.O.C.  
BLOCK DIAGRAM  
Ares-1  
Rev. 1.0, March 18, 2019

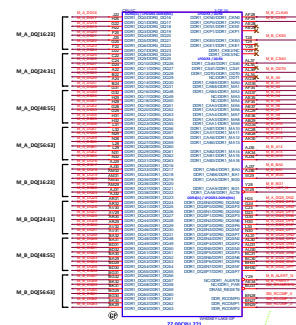
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CPU1 will use IOM control to Whiskeylake-U



**Layout Notes:**

#65729 Rev 1.0  
CNU-U DDR4 x16 Memory Down Routing Guideline (m2)

Design Guideline:  
SM\_RCOMP\_S/U2 keep routing length less than 500 mils

#65729 Rev 1.0  
CNU-U DDR4 x16 Memory Down Routing Guideline (m2)

DDR\_RCOMP: 12500 x1% on plug to V50  
DDR\_RCOMP[S1]: 80.50 x1% on plug to V50  
DDR\_RCOMP[S2]: 10000 x1% on plug to V50

PCH strap pin: [CFG3](#) [CFG4](#)

15,29    CFG3        CFG3  
15    CFG4

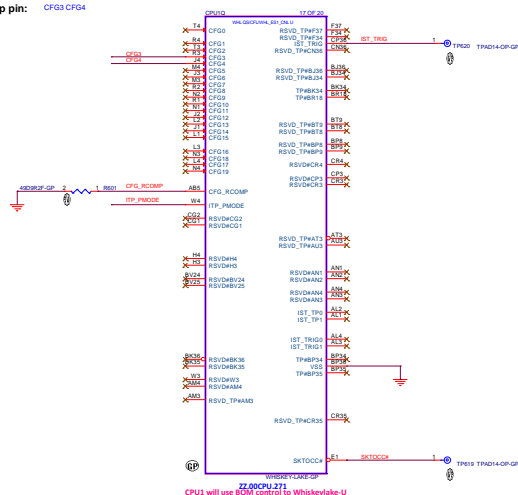
15,29  
15

CFG3  
CFG4

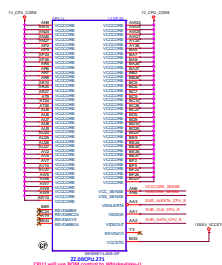
CFG3  
CFG4

```
99  IFP_PMODE <<<_____
```

```
99  IFP_PMODE <<<_____
```



ZZ.00CPU.271  
CPU1 will use BOM control to Whiskeylake-L



CPU1 will use BOM control to Whiskeylake-U

**Layout Note:**  
The total length of Data and Clock (from CPU to each VE) must be equal (+0.2 inch). Route the Signal along between the Clock and the Data signals.

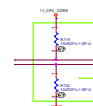
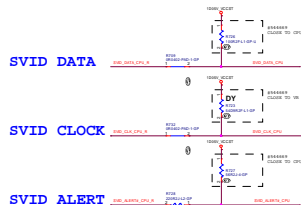


Figure 10-7. Routing Illustration for SVID Topology

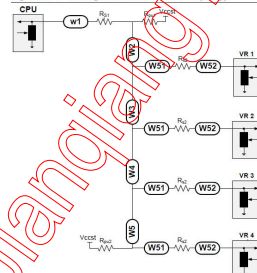


Table 10-10. SVID Bus Routing Guidelines

System	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>501</sub> [°]	R <sub>502</sub> [°]	R <sub>51</sub> [°]	R <sub>52</sub> [°]	W <sub>53</sub> [°]
WDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.4
WDSCK							Empty	45	0	50	
WDSALERT							56	Empt	220	0	





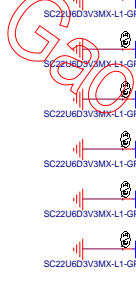
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LAR-1		
<div>緯創資通Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleCPU (RSVD)		
SizeA4	Document NumberAres-1	Rev-1M
Date: Thursday, March 19, 2020		Sheet 9 of 99

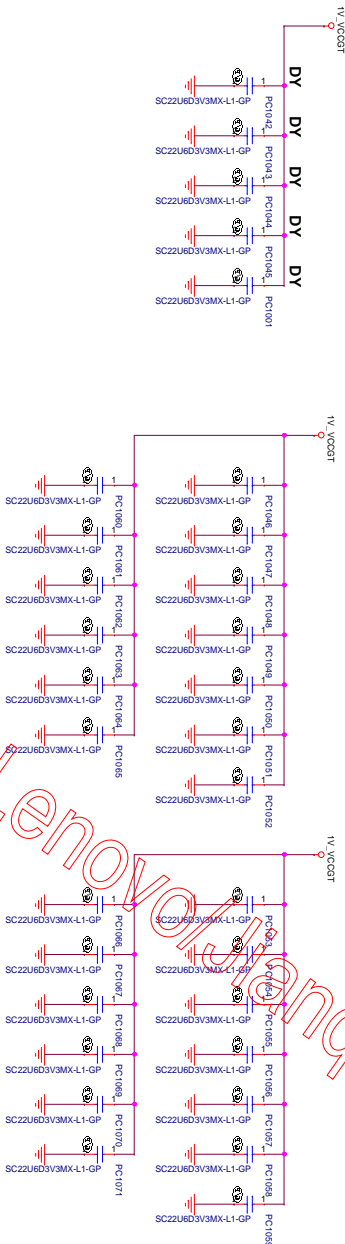
```
U42
IccMax current-10ms max = 70 mA
```

22uF	PCS	Cap
U42	35	330uF*2
U22	22	330uF*1



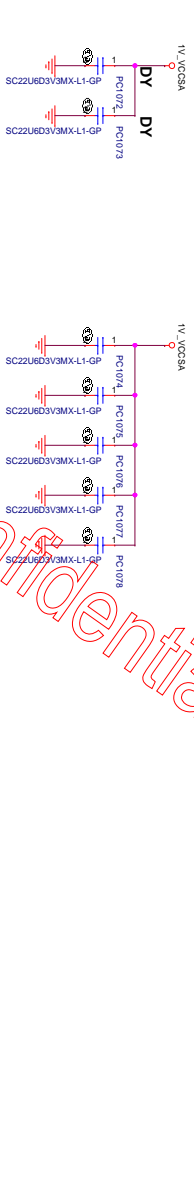
## CMT\_U42

22uF	PCS	Cap
CML	26	330uF*1



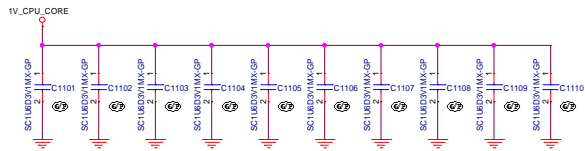
## CMT\_U42

```
U42
IccMax current-10ms max = 5 A
```

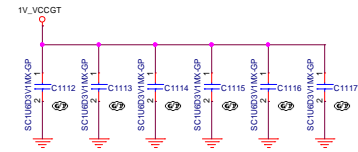


LBR-1	
緯創資通 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin-TaiWp Rd., Taipei Taipei/Hsin-TaiWp 221, Taiwan, R.O.C.	
<b>Title</b> <b>CPU (POWER CAP)</b>	<b>Docu. Number</b> <b>Ares-1</b>
<b>Size</b> 2060	<b>Doc. Date</b> THURSDAY, MARCH 31, 2005
<b>Model</b> 2060	<b>Size</b> 10
<b>Rev</b> -1M	<b>Doc. No.</b> 92

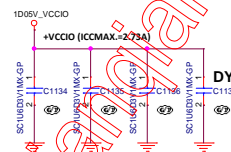
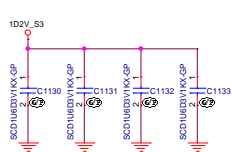
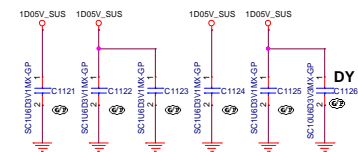
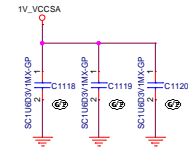
## VCORE WHL U42



## VCCGT WHL U42



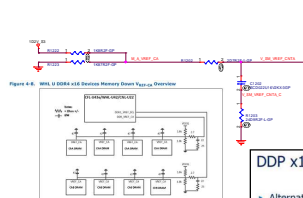
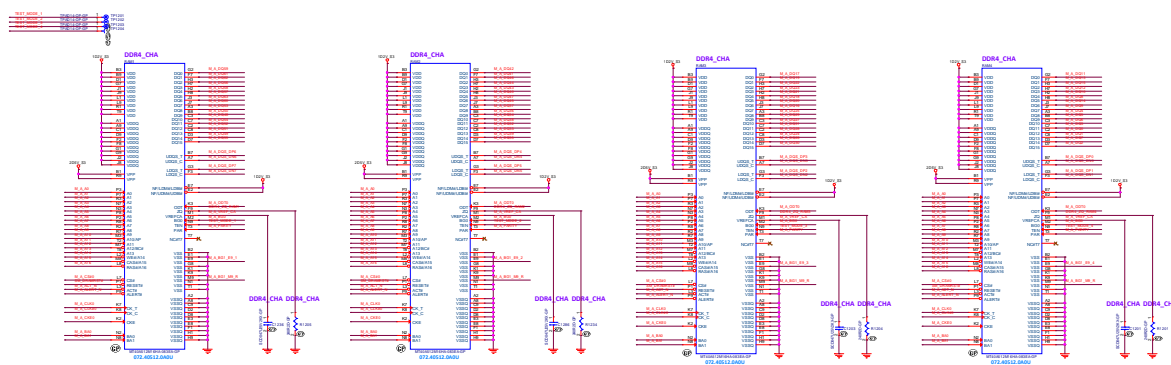
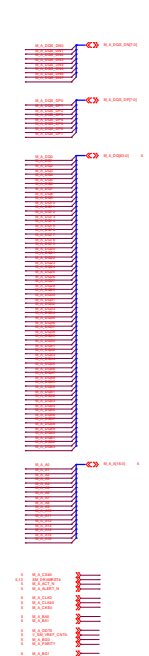
## VCCSA WHL U42



LAR-1

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (POWER CAP2)		
Size	Document Number	Rev
A3	Ares-1	-1M
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## SDP &amp; DDP SETTING

SDP-0: 0x1000

SDP-1: 0x1000

SDP-2: 0x1000

SDP-3: 0x1000

SDP-4: 0x1000

SDP-5: 0x1000

SDP-6: 0x1000

SDP-7: 0x1000

SDP-8: 0x1000

SDP-9: 0x1000

SDP-10: 0x1000

SDP-11: 0x1000

SDP-12: 0x1000

SDP-13: 0x1000

SDP-14: 0x1000

SDP-15: 0x1000

SDP-16: 0x1000

SDP-17: 0x1000

SDP-18: 0x1000

SDP-19: 0x1000

SDP-20: 0x1000

SDP-21: 0x1000

SDP-22: 0x1000

SDP-23: 0x1000

SDP-24: 0x1000

SDP-25: 0x1000

SDP-26: 0x1000

SDP-27: 0x1000

SDP-28: 0x1000

SDP-29: 0x1000

SDP-30: 0x1000

SDP-31: 0x1000

SDP-32: 0x1000

SDP-33: 0x1000

SDP-34: 0x1000

SDP-35: 0x1000

SDP-36: 0x1000

SDP-37: 0x1000

SDP-38: 0x1000

SDP-39: 0x1000

SDP-40: 0x1000

SDP-41: 0x1000

SDP-42: 0x1000

SDP-43: 0x1000

SDP-44: 0x1000

SDP-45: 0x1000

SDP-46: 0x1000

SDP-47: 0x1000

SDP-48: 0x1000

SDP-49: 0x1000

SDP-50: 0x1000

SDP-51: 0x1000

SDP-52: 0x1000

SDP-53: 0x1000

SDP-54: 0x1000

SDP-55: 0x1000

SDP-56: 0x1000

SDP-57: 0x1000

SDP-58: 0x1000

SDP-59: 0x1000

SDP-60: 0x1000

SDP-61: 0x1000

SDP-62: 0x1000

SDP-63: 0x1000

SDP-64: 0x1000

SDP-65: 0x1000

SDP-66: 0x1000

SDP-67: 0x1000

SDP-68: 0x1000

SDP-69: 0x1000

SDP-70: 0x1000

SDP-71: 0x1000

SDP-72: 0x1000

SDP-73: 0x1000

SDP-74: 0x1000

SDP-75: 0x1000

SDP-76: 0x1000

SDP-77: 0x1000

SDP-78: 0x1000

SDP-79: 0x1000

SDP-80: 0x1000

SDP-81: 0x1000

SDP-82: 0x1000

SDP-83: 0x1000

SDP-84: 0x1000

SDP-85: 0x1000

SDP-86: 0x1000

SDP-87: 0x1000

SDP-88: 0x1000

SDP-89: 0x1000

SDP-90: 0x1000

SDP-91: 0x1000

SDP-92: 0x1000

SDP-93: 0x1000

SDP-94: 0x1000

SDP-95: 0x1000

SDP-96: 0x1000

SDP-97: 0x1000

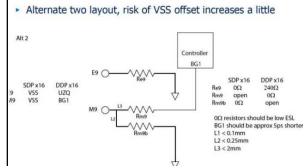
SDP-98: 0x1000

SDP-99: 0x1000

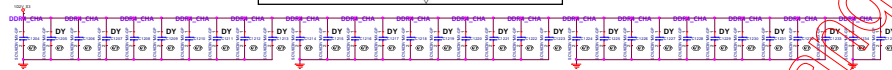
SDP-100: 0x1000

## DDP x16 and SDP x16 Compatible Layout

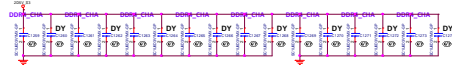
- Alternate two layout, risk of VSS offset increases a little



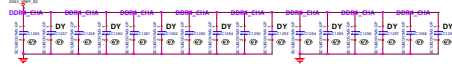
## VDDQ/VDD 1uF x16



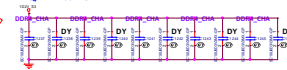
## VPP 1uF x8



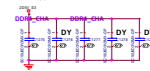
## VTT 1uF x8



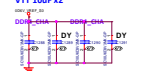
## VDDQ/VDD 10uF x5



## VPP 10uF x2



## VTT 10uF x2



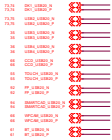
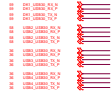
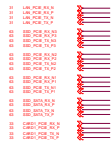


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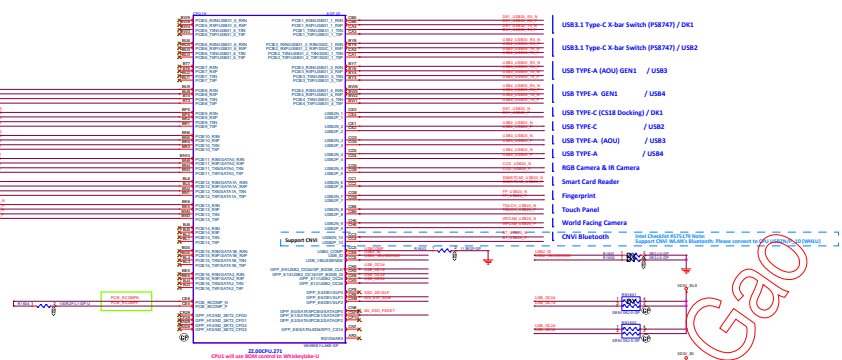
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LAR-1		
緯創資通		Wistron Corporation
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title DDR (RSVD)		
Size A4	Document Number Ares-1	Rev -1M
Date: Thursday, March 19, 2020		Sheet 14 of 99





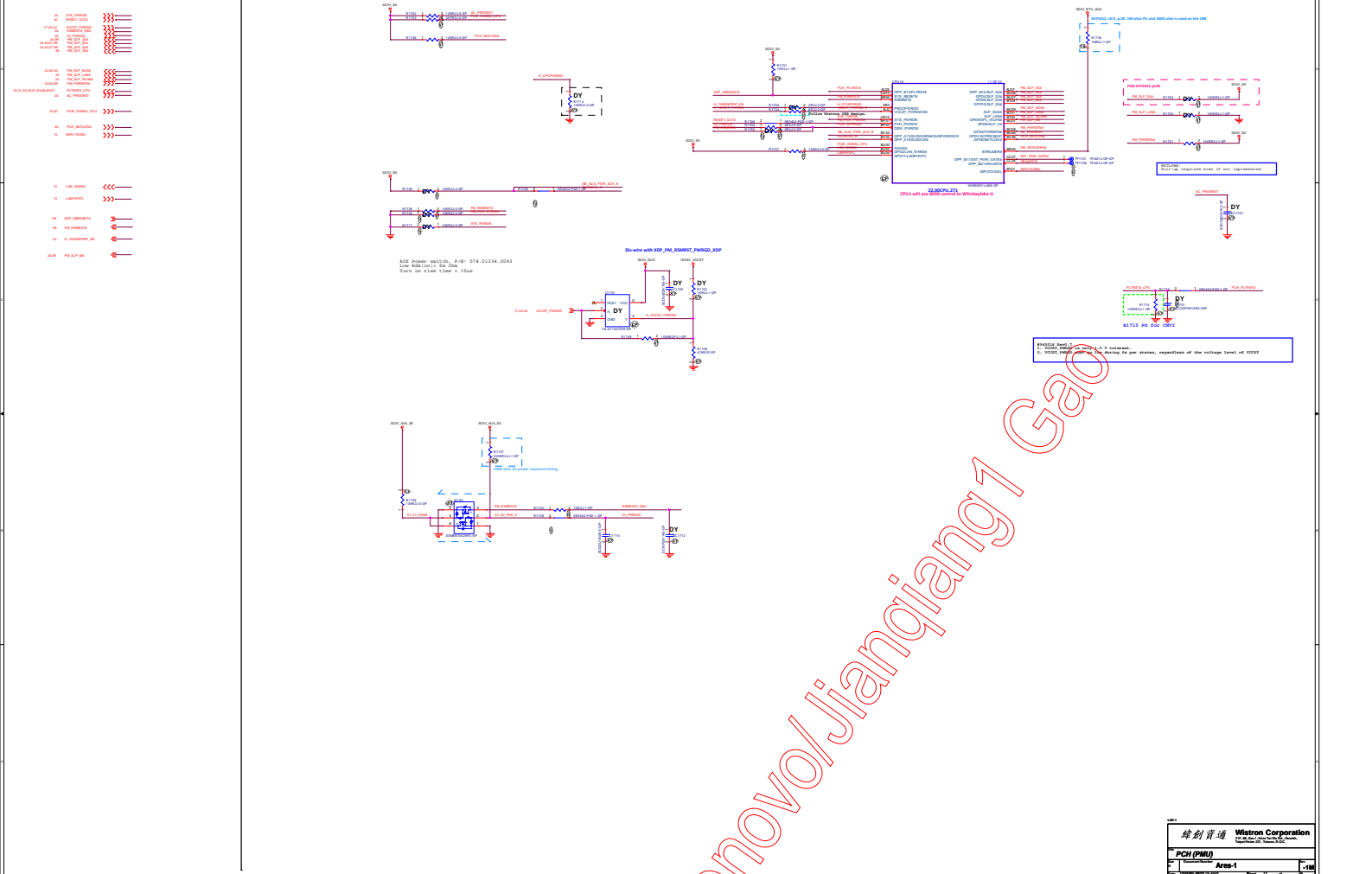
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M.2 PCIe SSD  
Media Card Reader

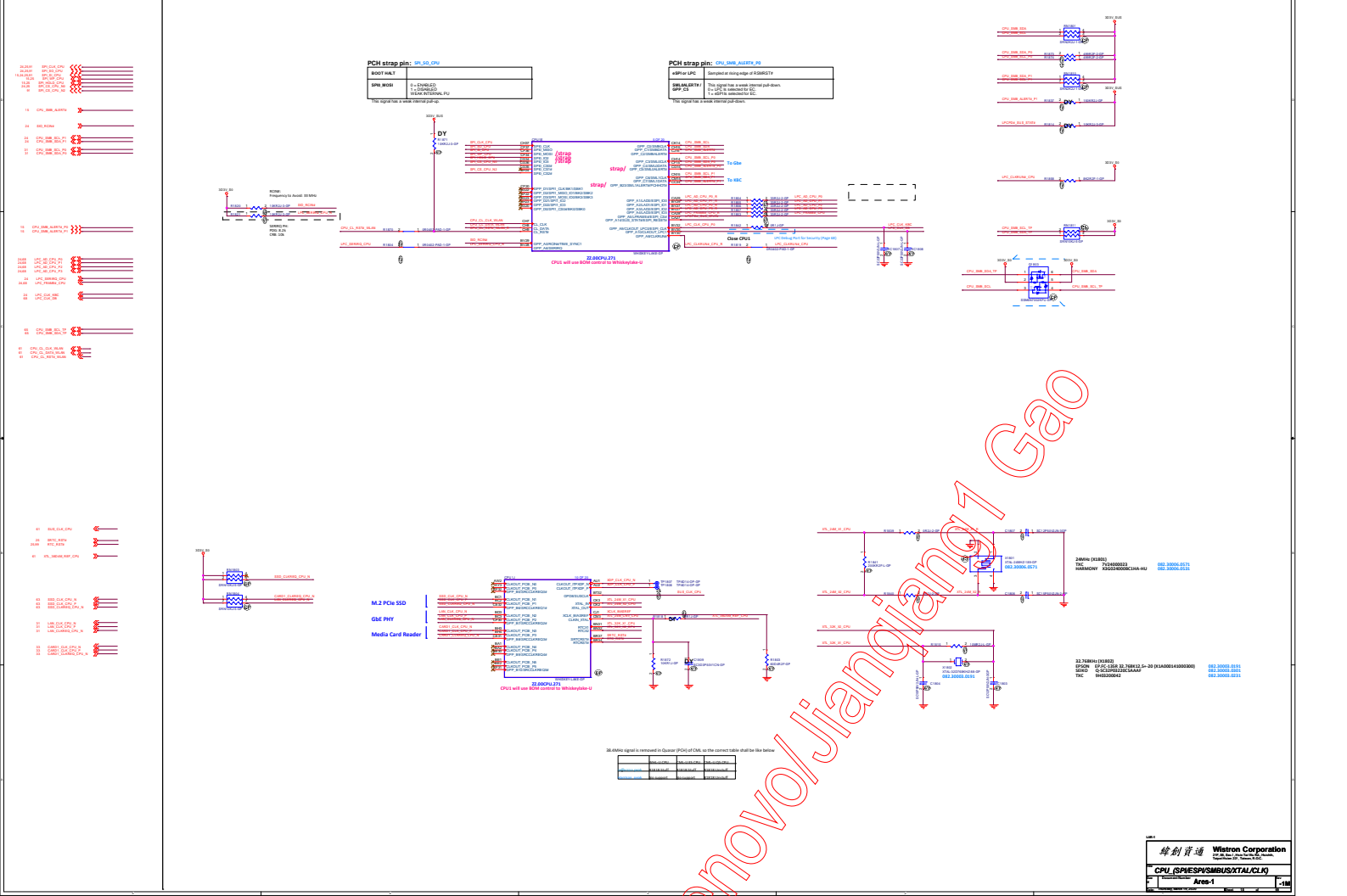


Legend Note:  
1. Orange Marked: A multi-pin connector (27 pins) is used.  
2. Blue Mark: A multi-pin connector (27 pins) is used.  
3. Green Mark: A multi-pin connector (27 pins) is used.

SATA Configuration		PCIe Configuration		USB 3.1 Configuration		USB 2.0 Configuration	
Port	Service	Port	Service	Port	Service	Port	Service
1	NC	1	NC	1	USB Type-C Port (USB Docking)	1	USB Type-C Port (USB Docking)
2	NC	2	NC	2	USB Type-A Port (ACU)	2	USB Type-A Port (ACU)
3	M.2 SATA SSD	3	NC	3	USB Type-A Port (ACU)	3	USB Type-A Port (ACU)
4	NC	4	NC	4	USB Type-A Port (ACU)	4	USB Type-A Port (ACU)
5	NC	5	NC	5	NC	5	Smart Card Reader
6	NC	6	NC	6	NC	6	Smart Card Reader
7	NC	7	NC	7	NC	7	World Facing Camera
8	NC	8	NC	8	NC	8	MicroSD Card Reader
9	NC	9	NC	9	NC	9	MicroSD Card Reader
10	NC	10	NC	10	NC	10	NC
11	NC	11	NC	11	NC	11	NC
12	NC	12	NC	12	NC	12	NC
13	NC	13	NC	13	NC	13	NC
14	NC	14	NC	14	NC	14	NC
15	NC	15	NC	15	NC	15	NC
16	NC	16	NC	16	NC	16	NC





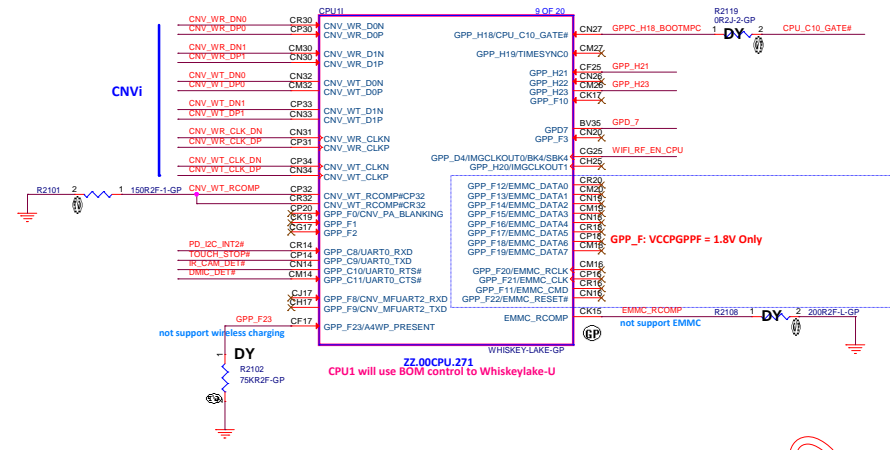


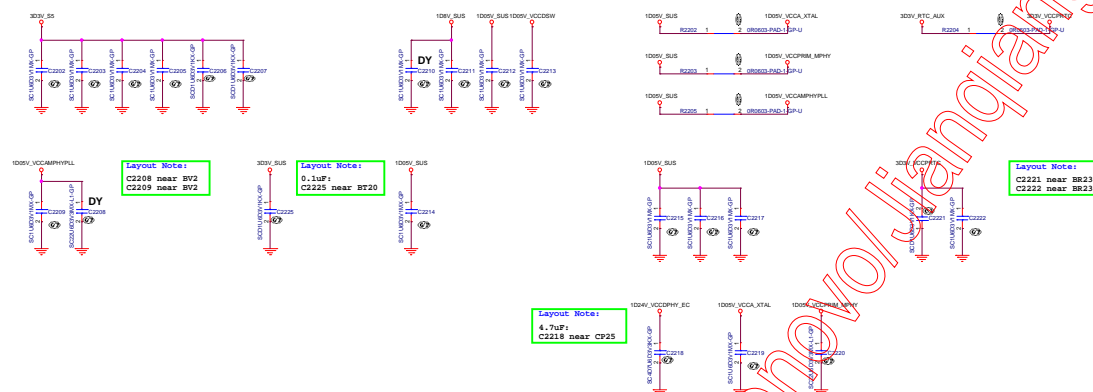
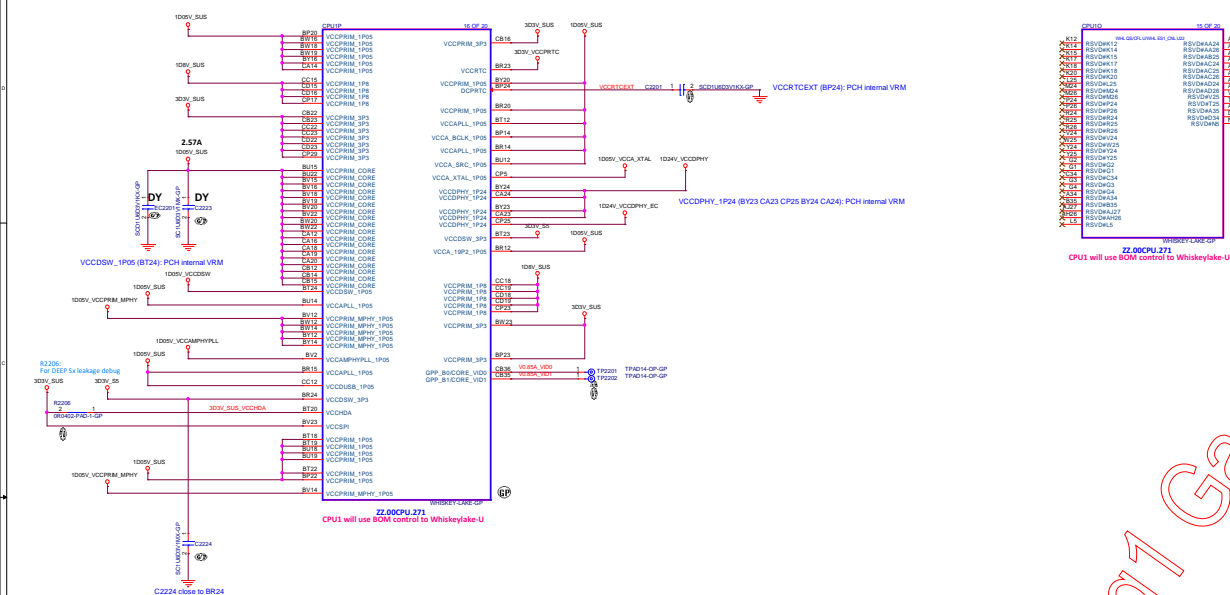
LAW-1		<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 808, Sec.1, Hsin Tai Wu Rd., Hsinchi, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CPU_(HDA/I2S/SD/DMIC)</b>			
Size	Docment Number	Rev	
A4		-1M	
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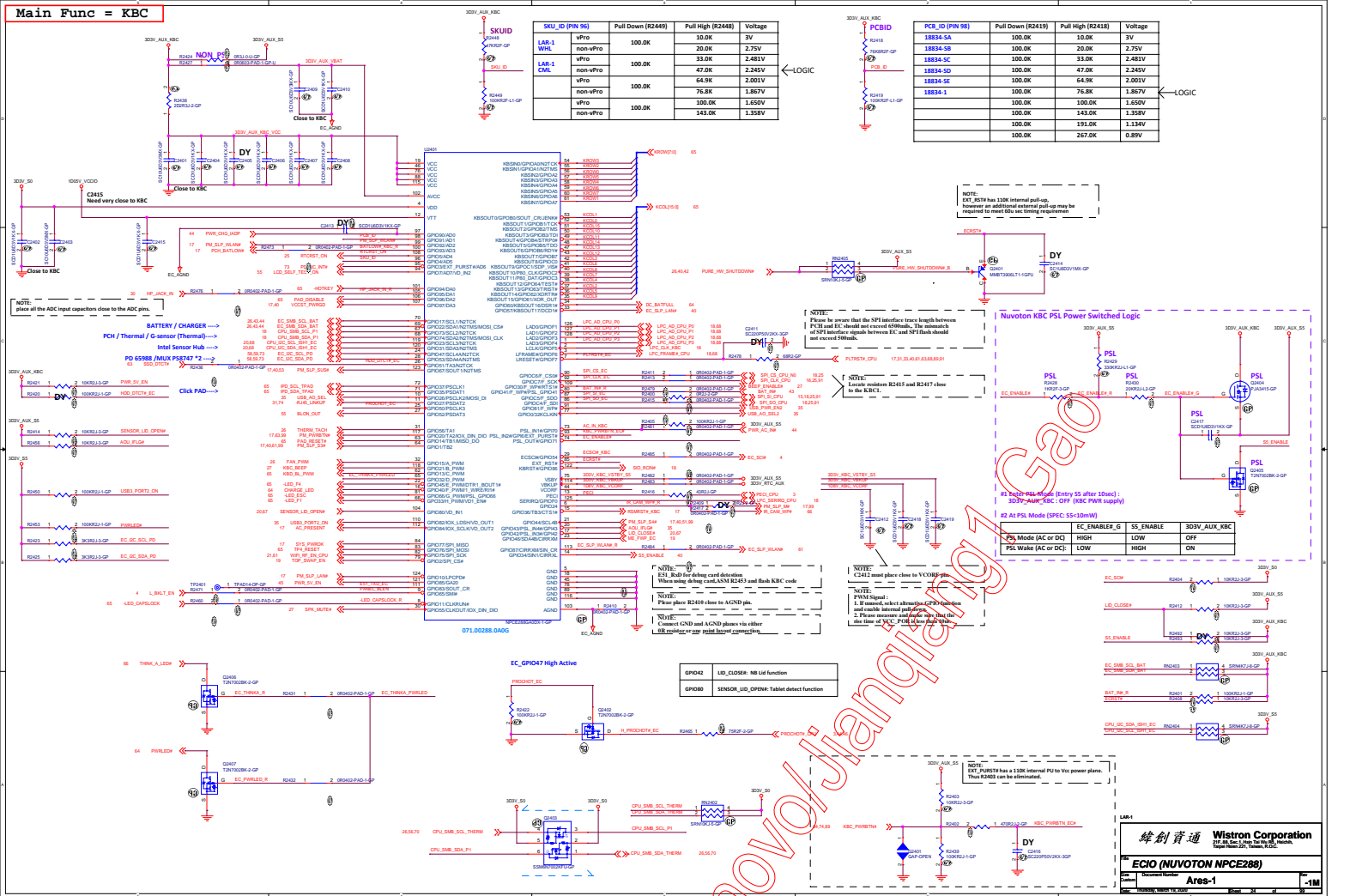
CNVi

- 61 CNV\_WT\_DN0
- 61 CNV\_WT\_DN0
- 61 CNV\_WT\_DP0
- 61 CNV\_WT\_DP1
- 61 CNV\_WT\_CLK\_DN
- 61 CNV\_WT\_CLK\_DP
- 61 CNV\_WR\_DN0
- 61 CNV\_WR\_DP0
- 61 CNV\_WR\_DN1
- 61 CNV\_WR\_DP1
- 61 CNV\_WR\_CLK\_DN
- 61 CNV\_WR\_CLK\_DP
- 73 PD\_ICC\_INT2#
- 55 TOUCH\_STOP#
- 66 IR\_CAM\_DET#
- 66 DMIC\_DET#
- 40 CPU\_C10\_GATE#
- 15 GPP\_H21
- 15 GPP\_H23
- 15 GPD\_7
- 24,61 WIFI\_RF\_EN\_CPU





CPU1T		20 DE 20	
N6	V56	CF23	V4
B37	V56	V4	V4
CB8	V56	CF24	V4
P10	V56	CF28	V4
B35	V56	V4	V4
CB1	V56	CF10	V3
P3	V56	V3	V3
CB4	V56	CF13	V3
CB4	V56	CF4	V4
P33	V56	V30	V3
T5	V56	V37	V3
CB7	V56	V3	V3
P36	V56	V37	V3
BA7	V56	BP30	V3
CC11	V56	V26	V3
CB8	V56	CF6	V3
BA28	V56	V27	V3
BA3	V56	CF31	V3
BA3	V56	V27	V3
CC20	V56	V27	V3
CB9	V56	CC25	V3
BB3	V56	V30	V3
CC25	V56	V30	V3
CB9	V56	CC25	V3
BB33	V56	V33	V3
CC25	V56	V33	V3
R29	V56	V35	V3
R29	V56	V35	V3
BB36	V56	BA26	V3
CC3	V56	V37	V3
R30	V56	V37	V3
BB3	V56	BP30	V3
CC7	V56	CC23	V3
R3	V56	BA32	V3
R3	V56	V37	V3
CC3	V56	BP30	V3
CC11	V56	BP33	V3
BB3	V56	BP33	V3
CC12	V56	BP35	V3
CC3	V56	BP35	V3
BB36	V56	BP19	V3
CC14	V56	BP16	V3
CC14	V56	BP19	V3
V33	V56	BP19	V3
CC16	V56	BP16	V3
CC16	V56	BP16	V3
T36	V56	CC14	V3
CC16	V56	CC14	V3
BP3	V56	CC14	V3
BP3	V56	CC14	V3
CF33	V56	CC14	V3
U26	V56	BP12	V3
BP3	V56	BP12	V3
CF35	V56	CC24	V3
CF35	V56	CC24	V3
BP3	V56	CC24	V3
BP33	V56	U24	V3
CF36	V56	BP7	V3
V3	V56	BA4	V3
BP35	V56	BA4	V3
BP35	V56	BA4	V3
CC3	V56	BA6	V3
Y27	V56	BA6	V3
BP36	V56	BA6	V3
BP3	V56	BA4	V3
V3	V56	BA4	V3
BP3	V56	BA4	V3
CF14	V56	BP3	V3
V30	V56	BP4	V3
BP3	V56	CC2	V3
CF19	V56	V35	V3
BP3	V56	V35	V3
BP29	V56	CCM	V3
CF2	V56	V35	V3
V3	V56	AC5	V3
BE3	V56	CC8	V3



SKU ID (PIN 56)	Pull Down (R2445)	Pull High (R2446)	Voltage
LAS-1 WHL	vPro	100.0K	18.0K 3V
LAS-1 CML	non-vPro	100.0K	20.0K 2.75V
	vPro	100.0K	33.0K 2.481V
	non-vPro	100.0K	47.0K 2.245V
	vPro	100.0K	64.0K 2.031V
	non-vPro	100.0K	76.8K 1.867V
	vPro	100.0K	100.0K 1.650V
	non-vPro	100.0K	143.0K 1.358V

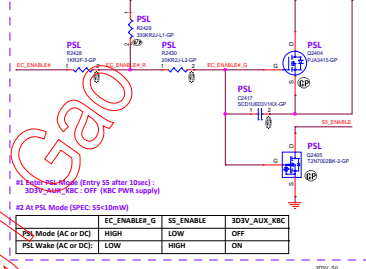
PCR ID (PIN 56)	Pull Down (R2419)	Pull High (R2418)	Voltage
18834-5A	100.0K	10.0K	3V
18834-5B	100.0K	20.0K	2.75V
18834-5C	100.0K	33.0K	2.481V
18834-5D	100.0K	47.0K	2.245V
18834-5E	100.0K	64.0K	2.031V
18834-1	100.0K	76.8K	1.867V
	100.0K	100.0K	1.650V
	100.0K	143.0K	1.358V
	100.0K	191.0K	1.134V
	100.0K	267.0K	0.89V

← LOGIC

NOTE: CAT\_0178 has 100K internal pull-up. However an additional internal pull-up may be required to meet 50u sec timing requirement

NOTE: Please be aware that the SPI interface trace length between P13 and EC should not exceed 400mm. The mismatch of SPI interface length between EC and SPI flash should not exceed 50mm.

Novotek KBC PSL Power Switched Logic



NOTE: CAT\_0178 has 100K internal pull-up. However an additional internal pull-up may be required to meet 50u sec timing requirement

NOTE: CAT\_0178 has 100K internal pull-up. However an additional internal pull-up may be required to meet 50u sec timing requirement

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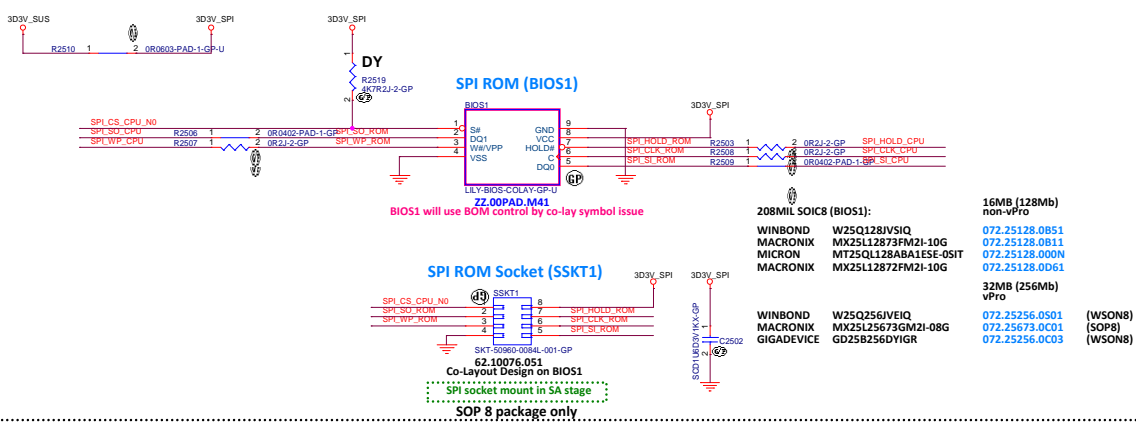
NOTE: CAT\_0178 has 100K internal pull-up. However an additional internal pull-up may be required to meet 50u sec timing requirement

Wistron Corporation  
ECIO (NUVOTON NPCE288)  
Ares-1  
-1M



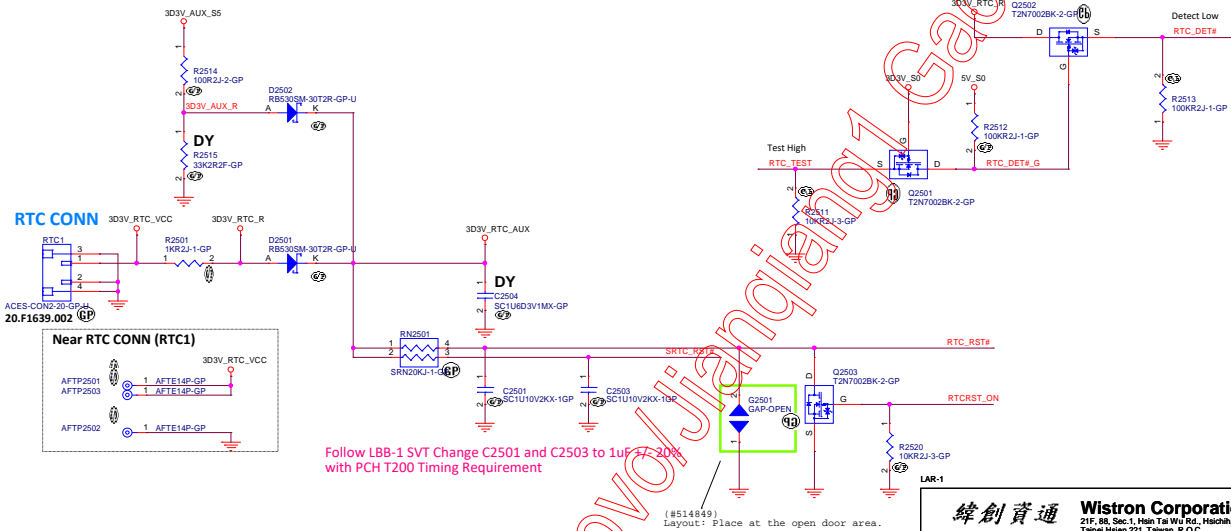
Main Func = SPI Flash

18,24	SPI_CS_CPU_N0	<<
18,24,91	SPI_CLK_CPU	<<
15,18,24,91	SPI_SI_CPU	<<
15,18	SPI_SD_CPU	<<
15,18	SPI_WP_CPU	<<
15,18	SPI_HOLD_CPU	<<



Main Func = RTC

18,99	RTC_RST#	<<
18	SRTC_RST#	<<
20	RTC_DET#	<<
18	RTC_TEST	<<
24	RTCRST_ON	<<

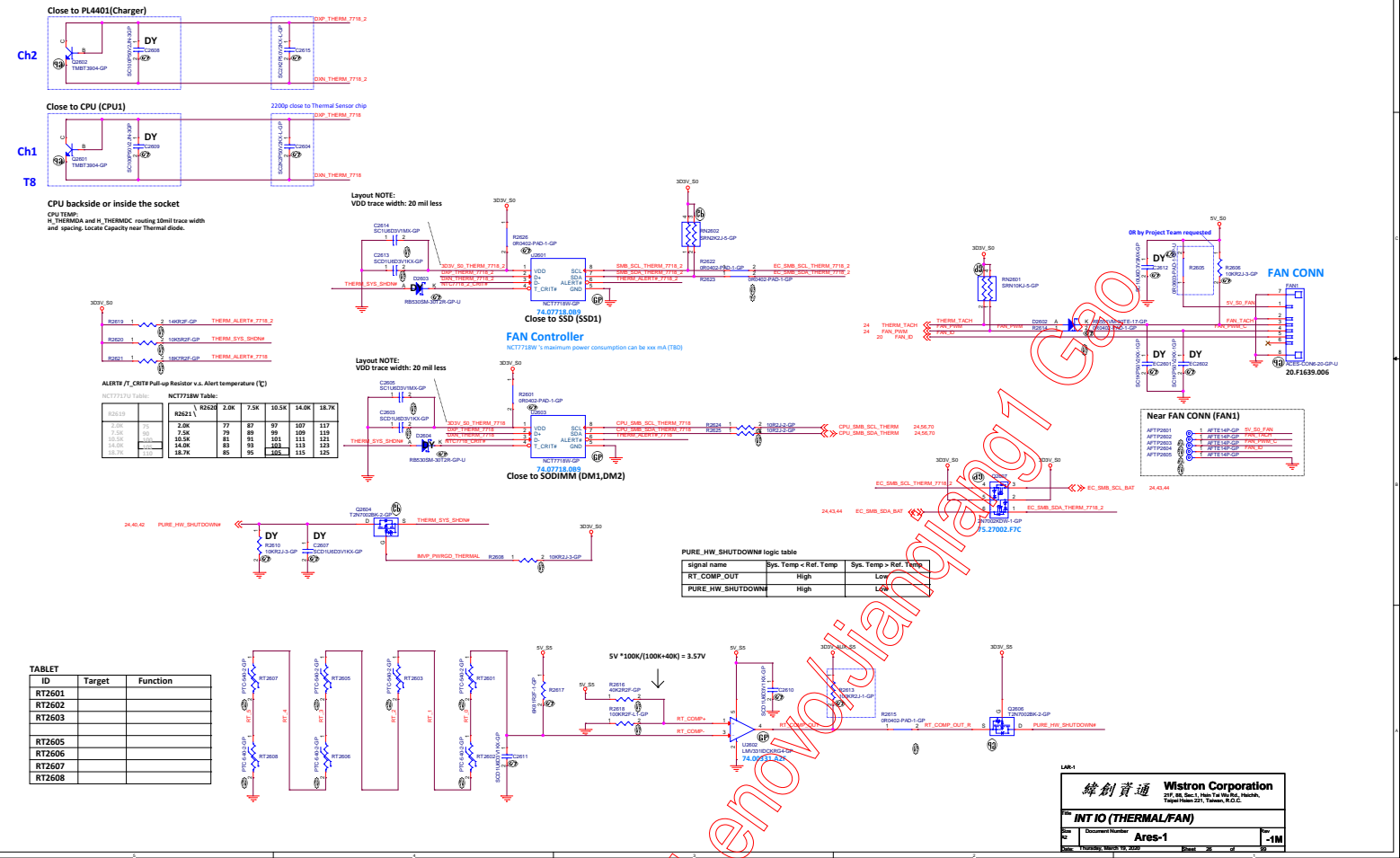


緯創資通 Wistron Corporation  
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File	FLASH/RTC		
Size	Document Number	Ares-1	Rev
			-1M
Date:	Thursday, March 19, 2020	Sheet	25 of 99

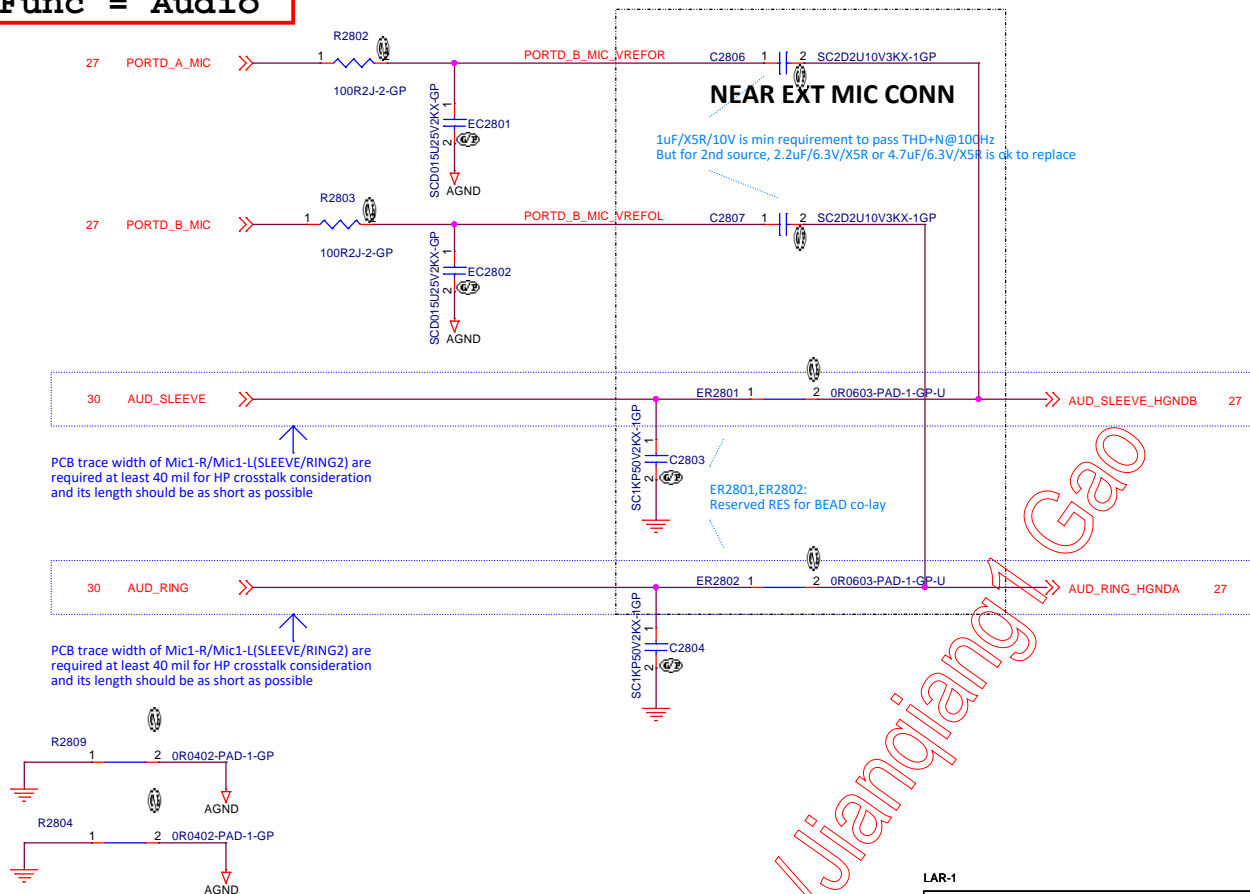
Thermal Sensor

Sensor	Target
U2601	SSO
U2603	DIMM
Q2601	CPU
Q2602	Charger





**Main Func = Audio**

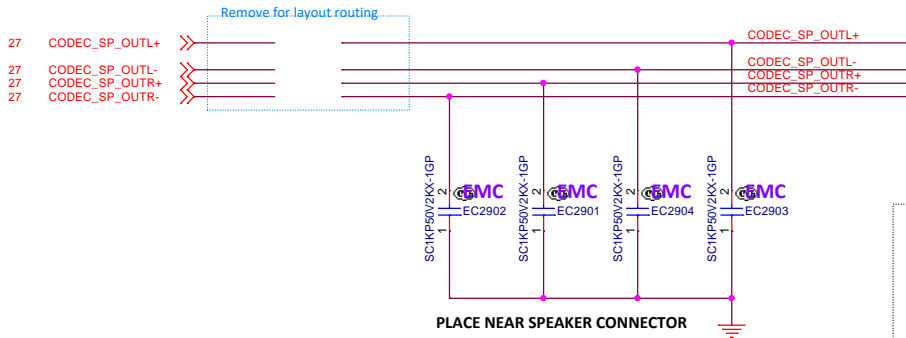


LAR-1

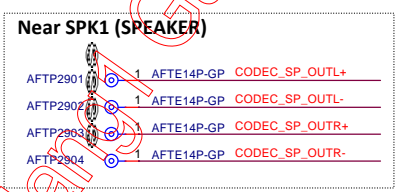
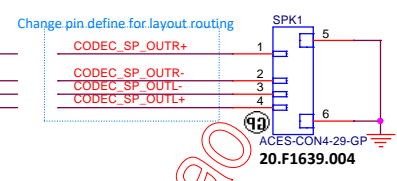
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>AUDIO (MIC I/F)</b>
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Size A4	Document Number <b>Ares-1</b>	Rev <b>-1M</b>
Date: Thursday, March 19, 2020	Sheet 28 of 99	

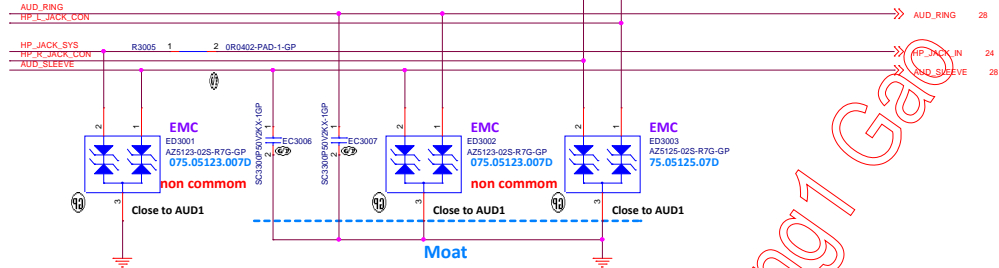
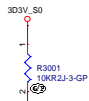
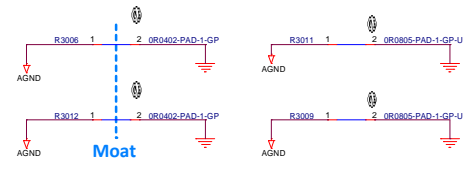


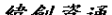
SPEAKER CONN

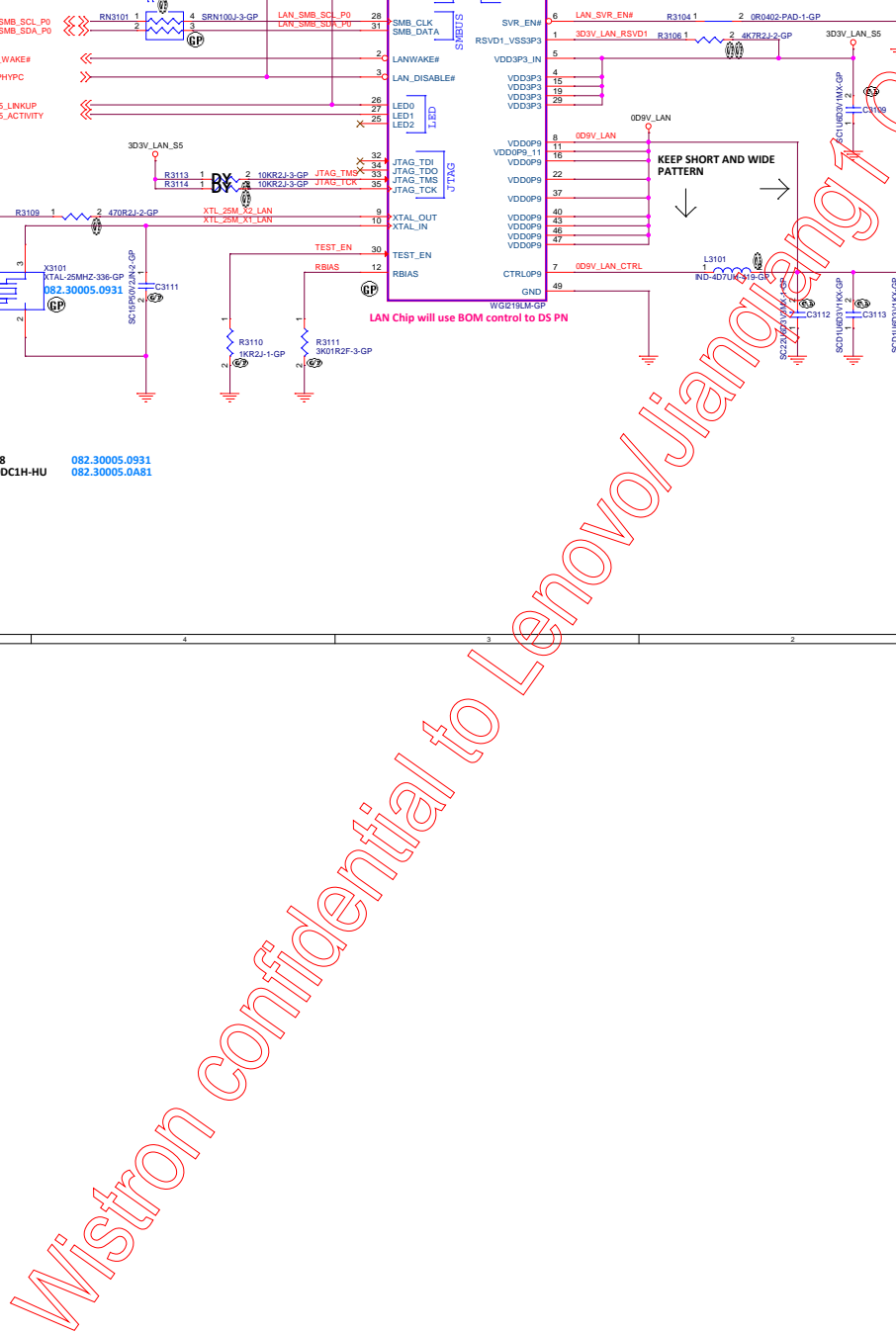


LAR-1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>AUDIO (SPEAKER)</b>			
Size A4	Document Number <b>Ares-1</b>		Rev <b>-1M</b>
Date: Thursday, March 19, 2020	2	Sheet 29 of 99	1



 <b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichai, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>AUDIO (AUDIO JACK)</b>			
<b>Size</b> A3	<b>Document Number</b> <b>Ares-1</b>		<b>Rev</b> <b>-1M</b>
<b>Date:</b> Thursday, March 19, 2020	<b>Sheet</b> 30	<b>of</b> 99	



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LAR-1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN (RSVD)			
Size	Document Number		Rev
A4	Ares-1		-1M
Date: Thursday, March 19, 2020		Sheet 32 of 99	
2		1	



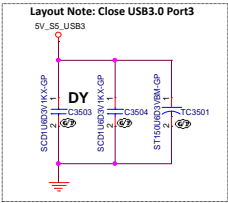
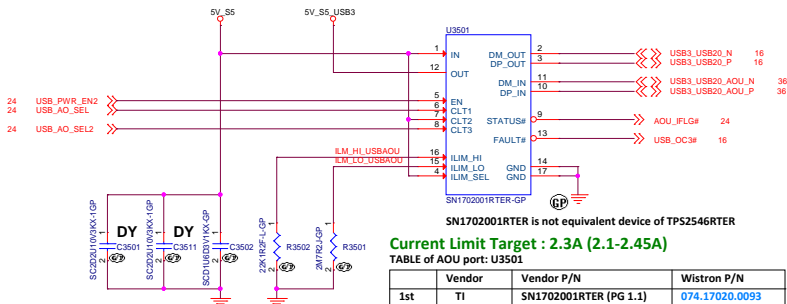


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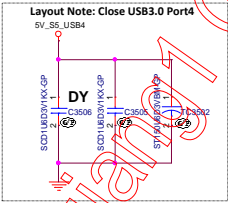
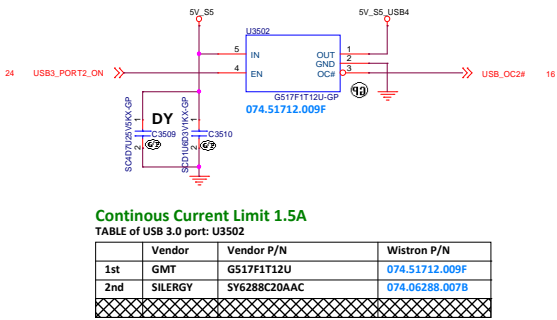
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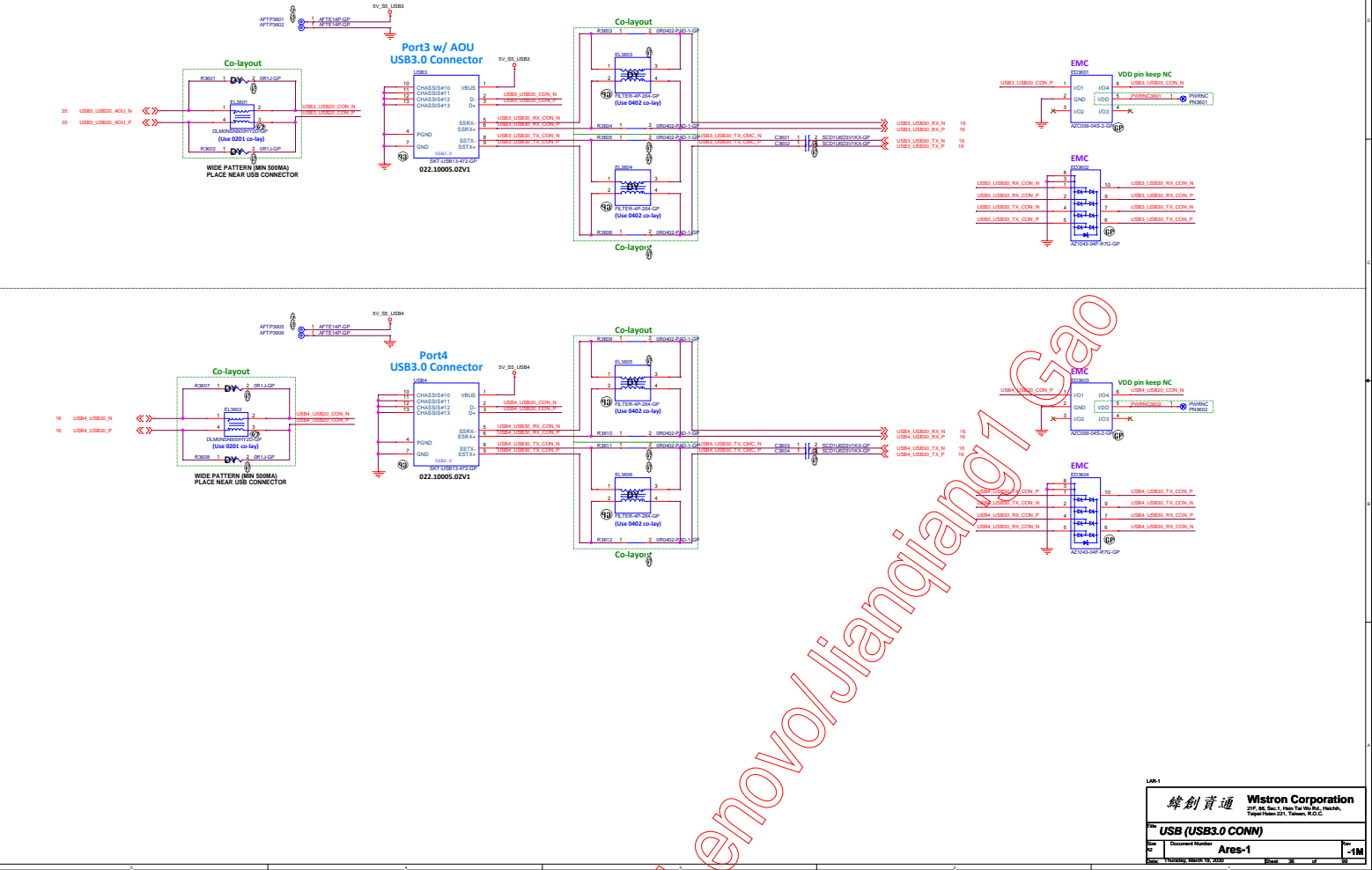
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TitleUSB (RSVD)	
SizeA4	Document NumberAres-1
Date: Thursday, March 19, 2020	Rev-1M
2	Sheet 34 of 99

For USB3.0 System Port3 (For AOU)



For USB3.0 System Port4





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LAR-1	
<div>緯創資通Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
TitleUSB (RSVD)	
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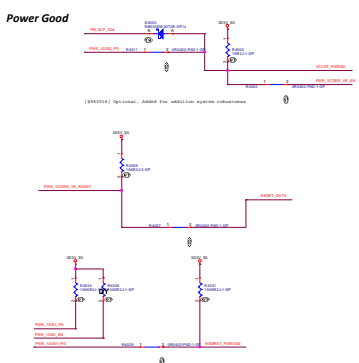
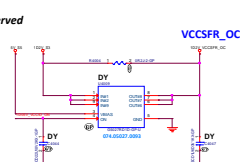
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SizeA4	Document NumberAres-1
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SizeA4	Document NumberAres-1
Date: Thursday, March 19, 2020	Rev-1M
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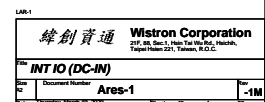




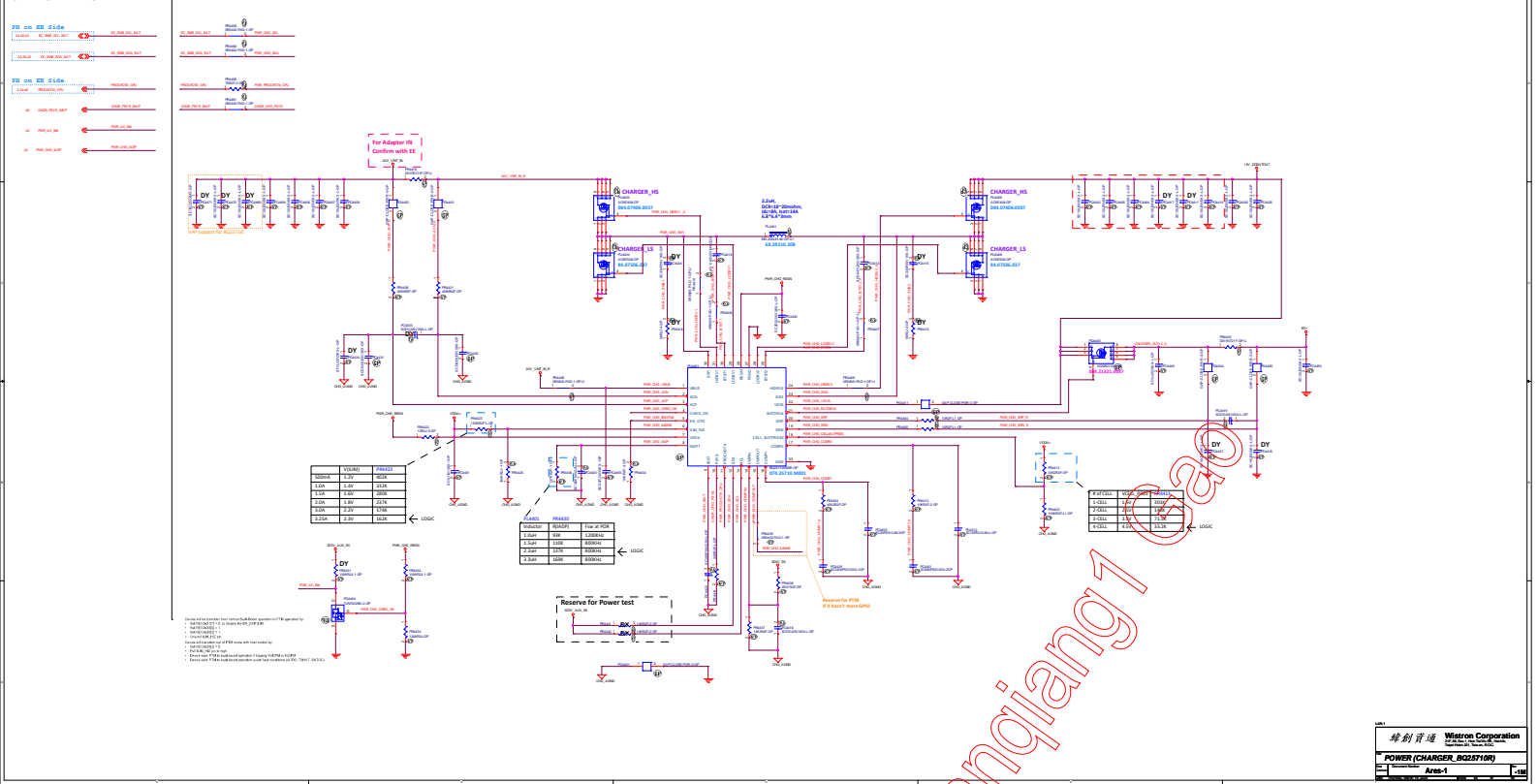
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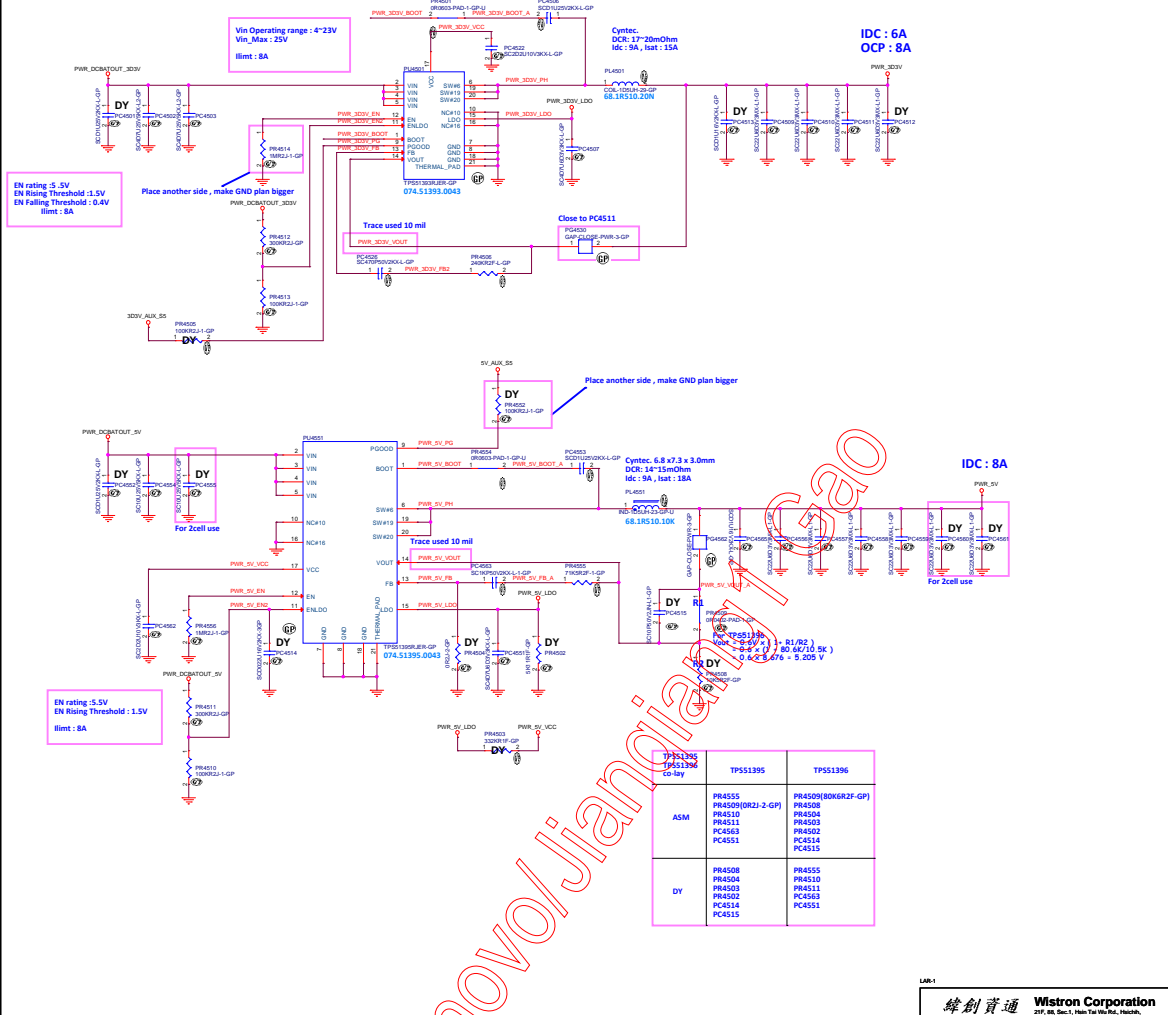
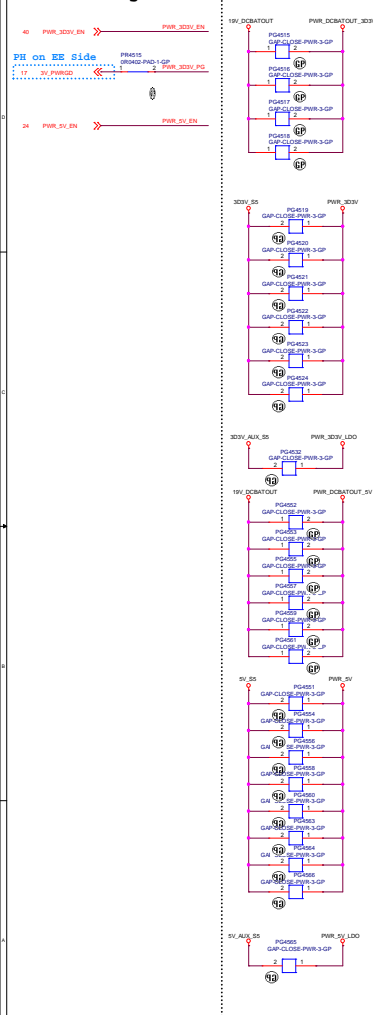
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SizeA4	Document NumberAres-1
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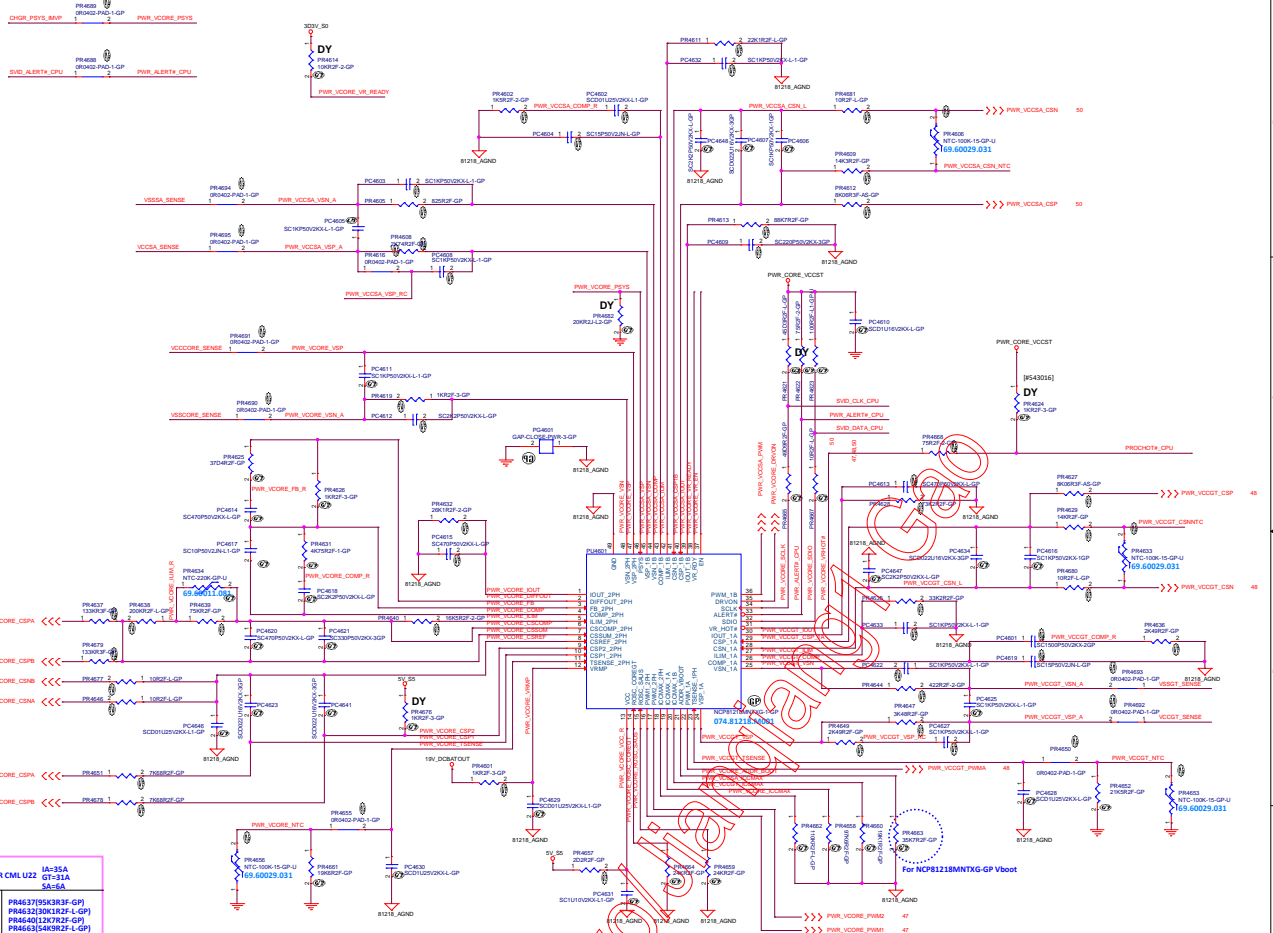
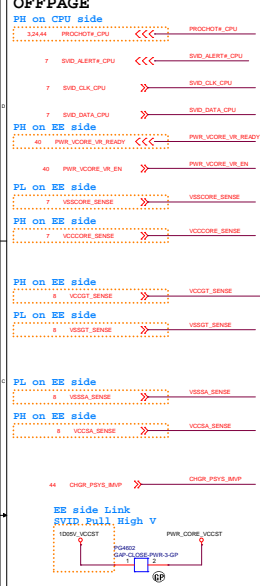
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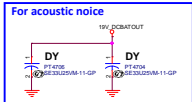
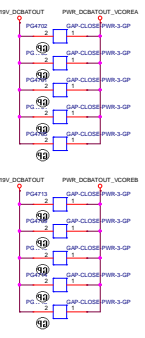


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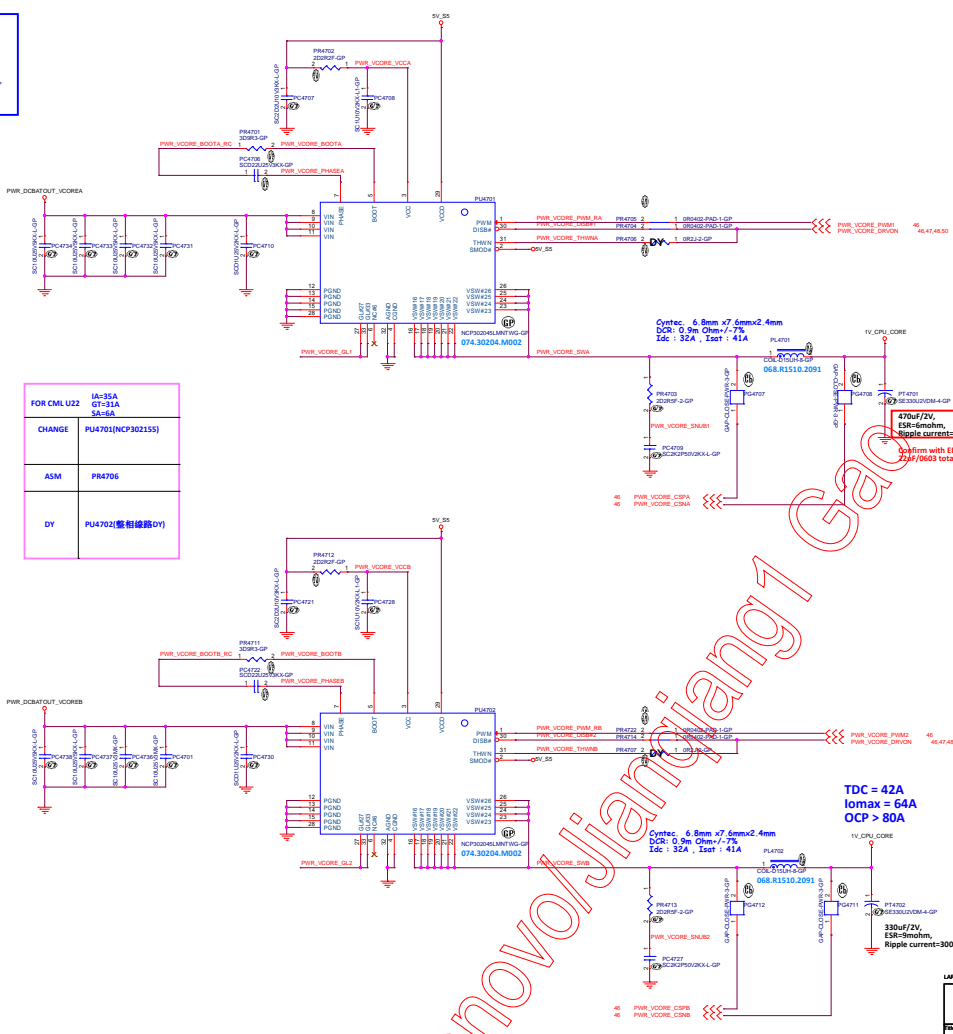


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CHANGE	PR4637[95K3R3F-GP] PR4632[30K1R2F-L-GP] PR4640[12K7R2F-GP] PR4663[54K9R2F-L-GP]	
ASM	PR4676	
DY	PR4679 PR4677 PC4641	

OFFPAGE



FOR CML U22	IA=35A GT=31A SA=5A
CHANGE	PU4701(NCP302155)
ASM	PR4706
DY	PU4702(雙相線路DY)



Cytech: 6.8mm x7.6mmx2.4mm  
DCR: 0.9m Ohm +/- 7%  
Isc: 32A, Isat: 41A

470uF/2V  
ESR=6mohm  
Ripple current=3000mA  
330uF/2V  
ESR=9mohm  
Ripple current=3000mA

TDC = 42A  
Iomax = 64A  
OCP > 80A

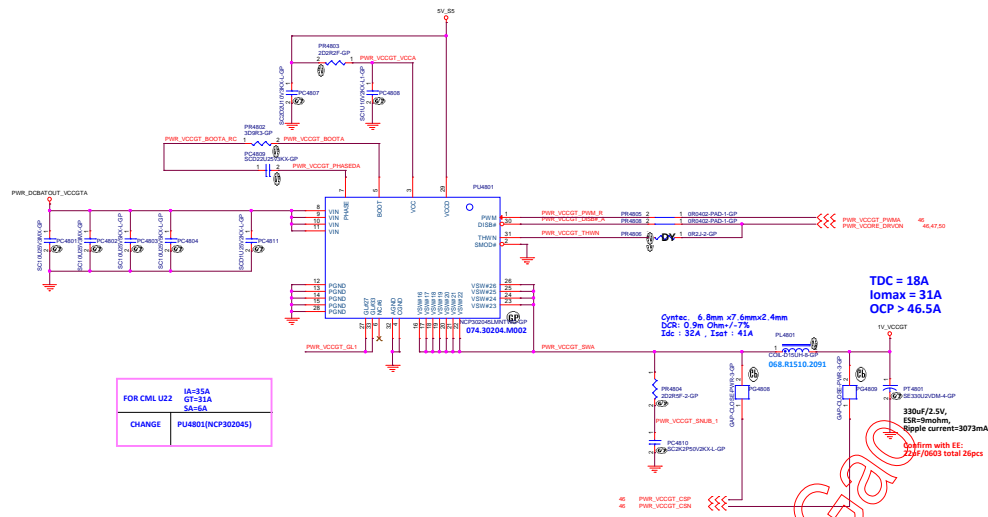
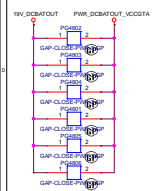
緯創資通 Wistron Corporation  
27F, 28, Sec. 2, Ping-Tai Highway, Taipei 105, Taiwan, R.O.C.

POWER (NCP302045LM\_VCORE)

Document Number Ares-1

Rev: 1.00 Date: 2023.10.20

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FOR CML U22		IA=35A GT=31A SA=6A
CHANGE	PU4801(NCP302045)	



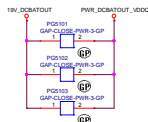
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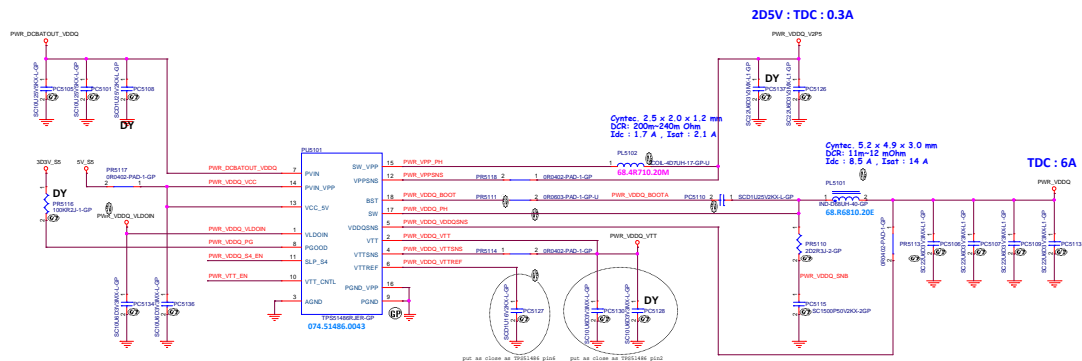
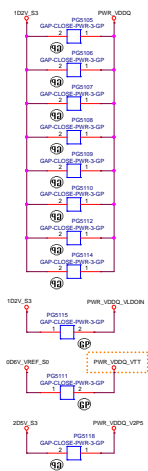
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TitlePOWER (RSVD)		
SizeA4	Document NumberAres-1	Rev-1M
Date: Thursday, March 19, 2020		Sheet 49 of 99



## OFFPAGE\_GAP



STATE	VTT_CNTL	SLP_S4	VFP	VDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

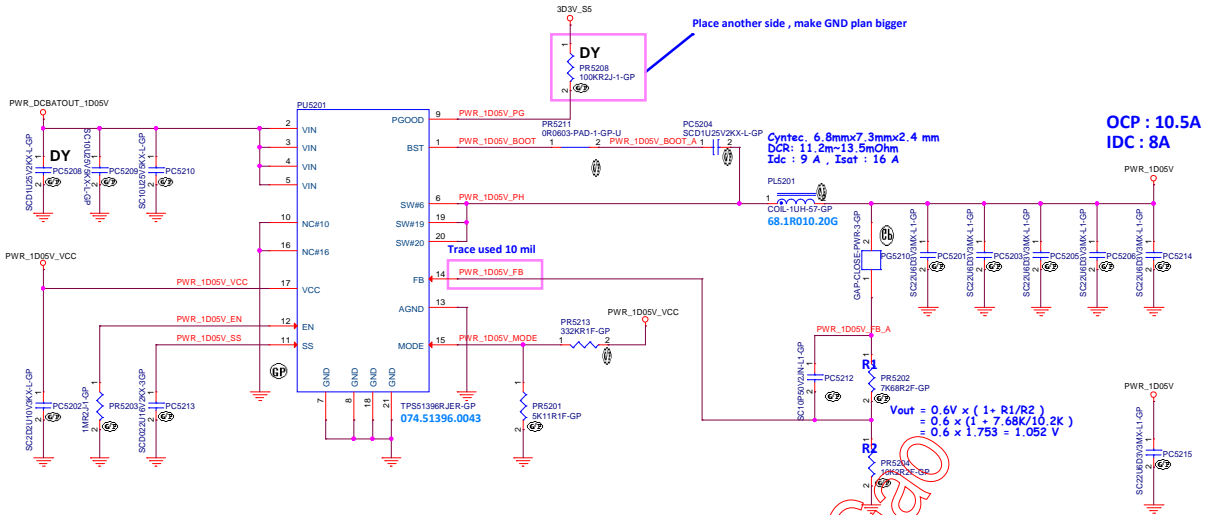
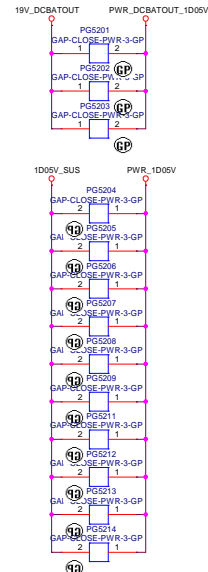


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PH on EE Side



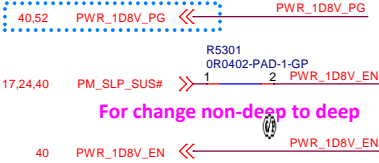
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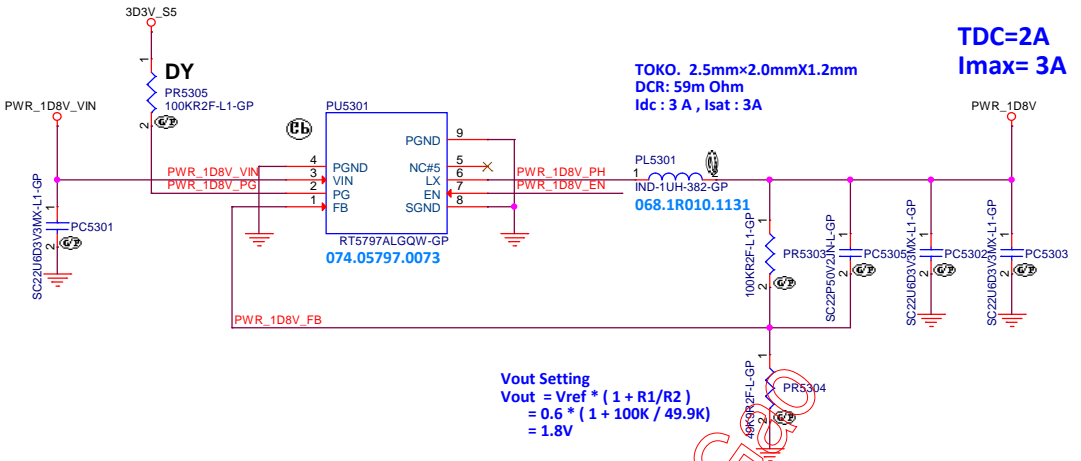
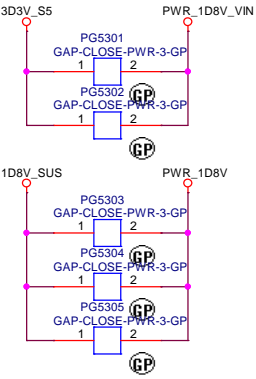
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title POWER (TPS51396_1D05V)	
Size A3	Document Number Ares-1
Date: Thursday, March 19, 2020	Sheet 52 of 59

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LAR-1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title POWER (RT5797\_1D8V)

Size A4 Document Number Ares-1 Rev -1M

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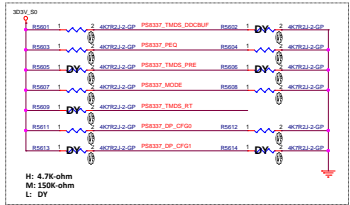
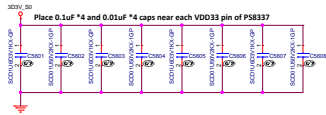
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TitlePOWER (RSVD)	
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TABLE 1: Automatic Switching Mode (CFG0 = H)  
SW (DDI\_PRIORITY1)  
L: USB Type-C has higher priority when both ports are plugged  
H: HDMI Port has higher priority when both ports are plugged  
Note: SW is pulled down with 150K-ohm internally

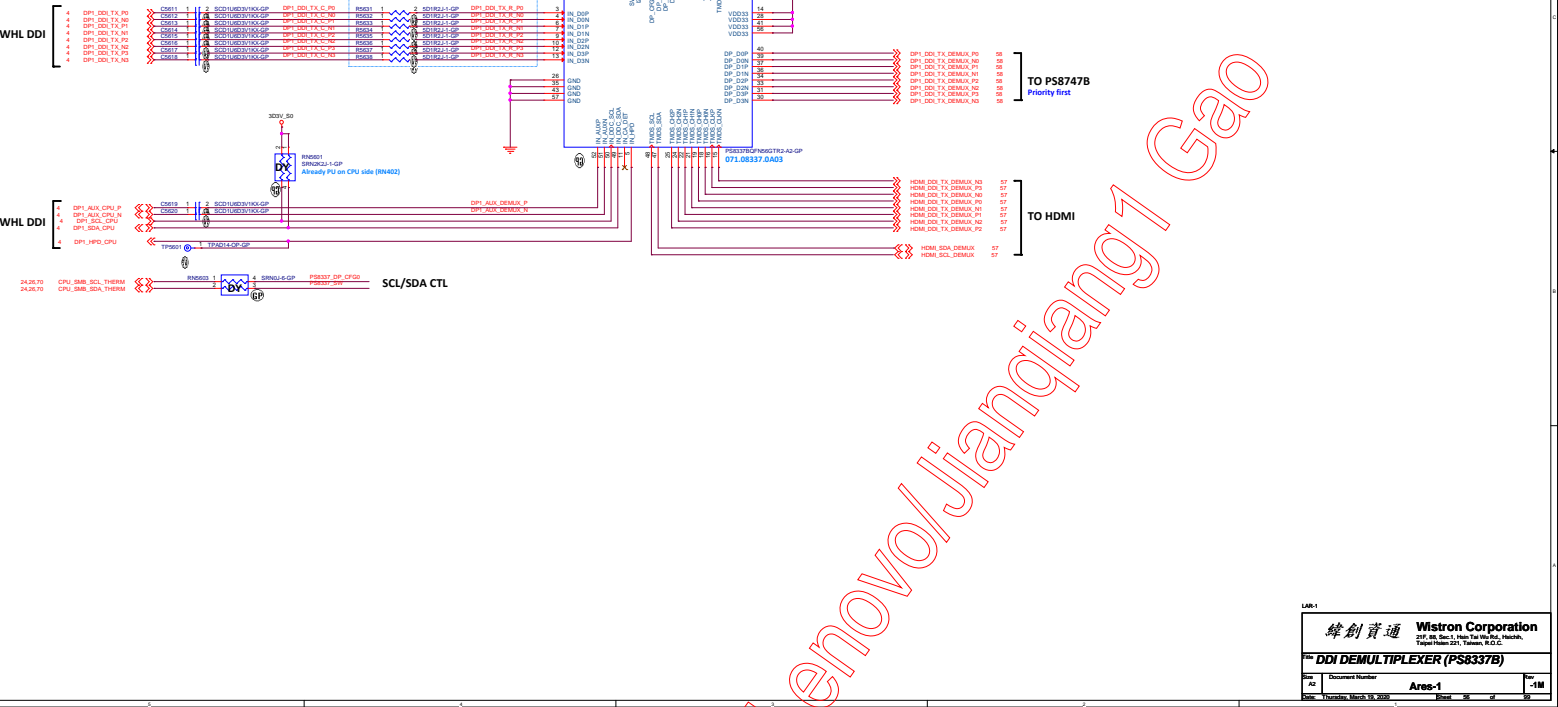


H: 4.7K-ohm  
M: 150K-ohm  
L: DY

WHL DDI

WHL DDI

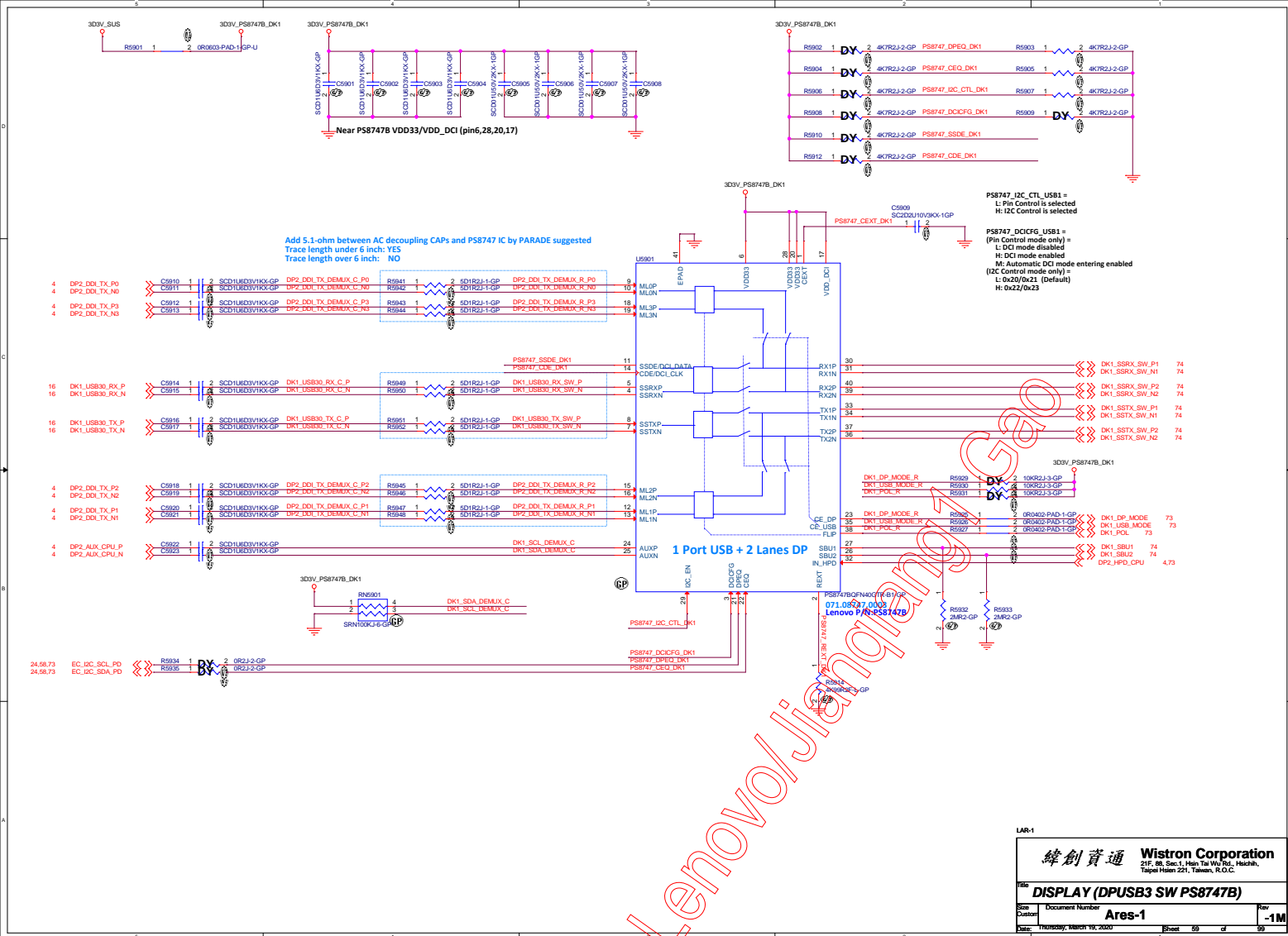
24.26.70 CPU\_SMB\_SCL\_THERM PS8337\_DP\_CFG0  
24.26.70 CPU\_SMB\_SDA\_THERM PS8337\_DP\_CFG1











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TitleINT IO (RSVD)	
SizeA4	Document NumberAres-1
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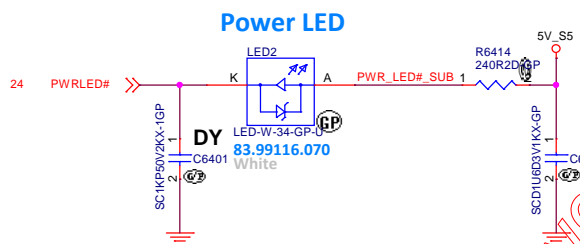
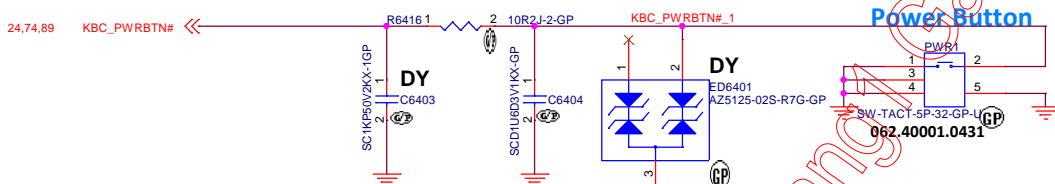
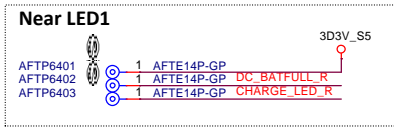
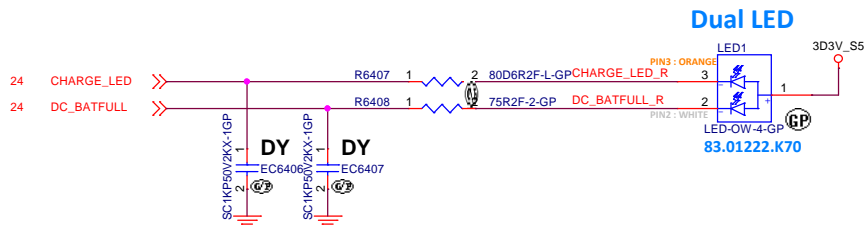


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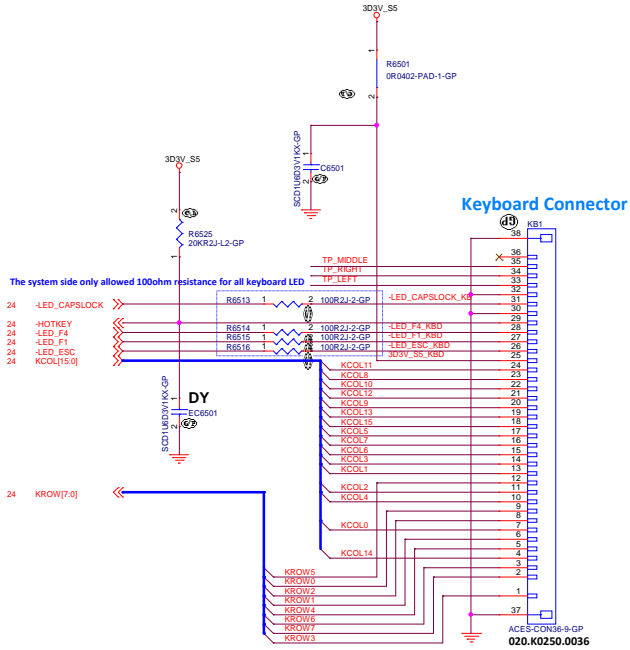
緯創資通 Wistron Corporation  
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Title LED/BTN/POWER BTN

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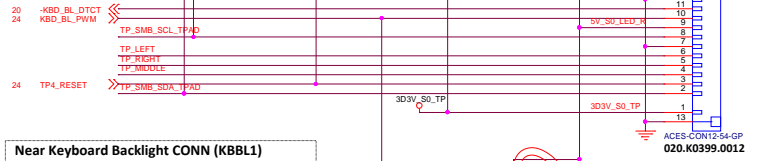


**Near Keyboard CONN (KB1)**  
Delete these test point for layout routing

**Near ClickPad CONN (TPAD1)**

AFTP6529	1	AFTE14P-GP	PAD_DISABLE
AFTP6521	1	AFTE14P-GP	IPD_SDA_TPAD
AFTP6522	1	AFTE14P-GP	IPD_SCL_TPAD
AFTP6523	1	AFTE14P-GP	PAD_RESET#
AFTP6524	1	AFTE14P-GP	3D3V_S0_CP_R
AFTP6525	1	AFTE14P-GP	CPU_SMB_SDA_TP
AFTP6526	1	AFTE14P-GP	TP_SMB_SCL_TPAD
AFTP6527	1	AFTE14P-GP	TP_SMB_SDA_TPAD
AFTP6531	1	AFTE14P-GP	CPU_SMB_SCL_TP
AFTP6528	1	AFTE14P-GP	

**Near Keyboard Backlight CONN (KBBL1)**  
Delete these test point for layout routing



**ClickPad Connector**



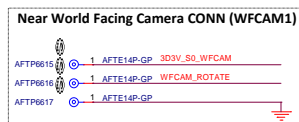
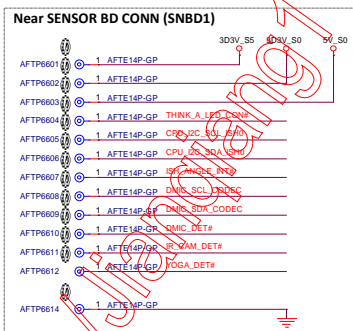
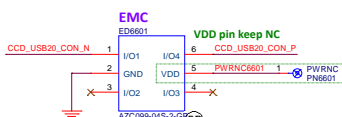
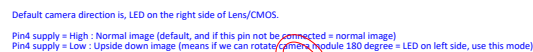
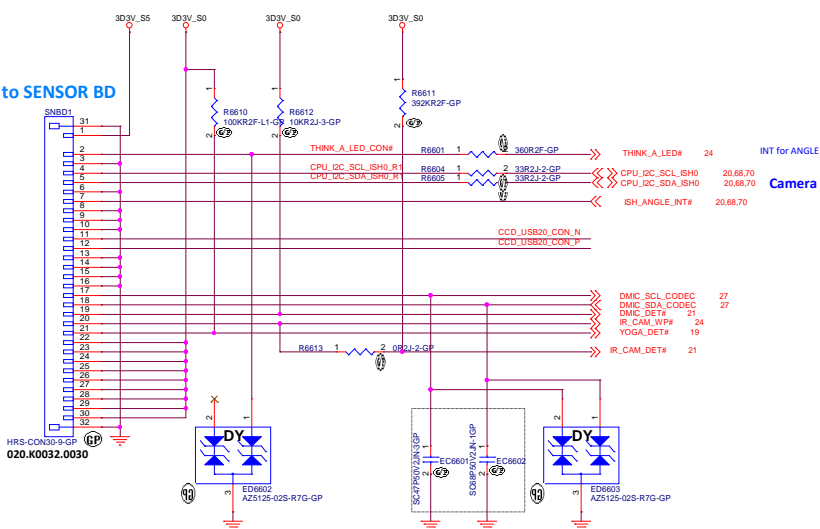
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Taipei Hsien 221, Taiwan, R.O.C.

File INT IO (KB/CP/TP)

Size A3 Document Number Ares-1 Rev -1M

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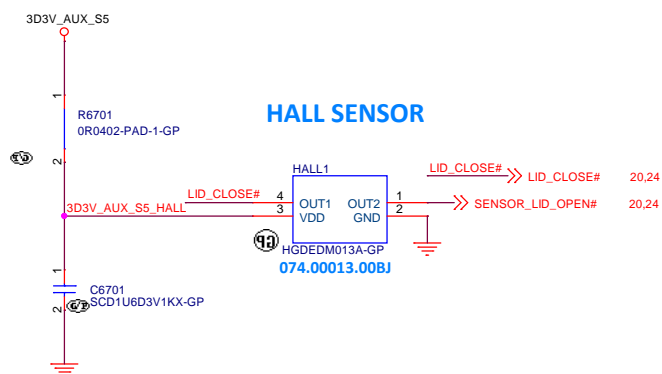
**LAR-1**

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Taipei Hsien 221, Taiwan, R.O.C.

Title **IO BOARD CONN (SNBD/WEGAM)**

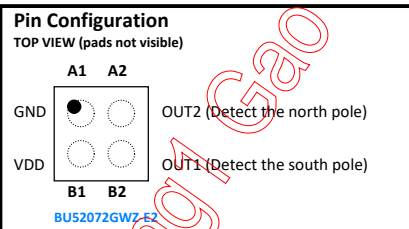
Size A3	Document Number <b>Ares-1</b>
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Pin1 need place at "Upper Right Corner"

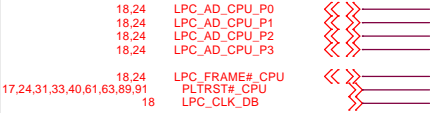
LID\_CLOSE# : NB Lid function  
SENSOR\_LID\_OPEN# : Tablet detect function



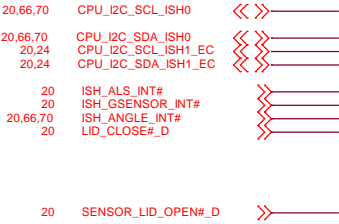
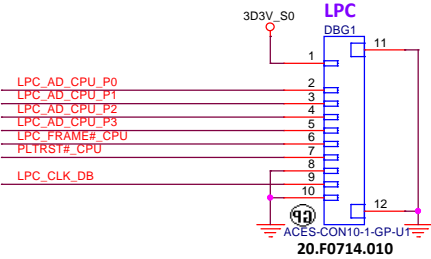
LAR-1

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<b>Title</b> <b>SENSOR (HALL-SENSOR)</b>	
<b>Size</b> A4	<b>Document Number</b> <b>Ares-1</b>
<b>Date</b> Thursday, March 19, 2020	<b>Rev</b> <b>-1M</b>
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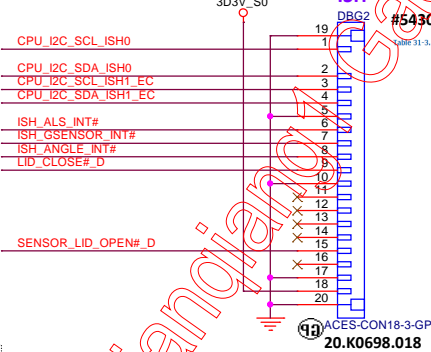
Main Func = Debug



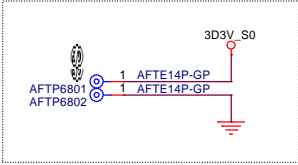
LPC Connector



Sensors Debug Hooks



Pin	Pin Function	Description
1	SPW_I2C0_SCL	Click line for the I2C0
2	SPW_I2C0_SDA	Click line for the I2C0
3	SPW_I2C1_SCL	Click line for the I2C1
4	SPW_I2C1_SDA	Click line for the I2C1
5	GND	System Ground
6	GPIOA[10]	Connect here one of the GPIOs in use
7	GPIOA[11]	Connect here one of the GPIOs in use
8	GPIOA[12]	Connect here one of the GPIOs in use
9	GPIOA[13]	Connect here one of the GPIOs in use
10	GND	System Ground
11	Reserved by Intel	Do not use
12	Reserved by Intel	Do not use
13	Reserved by Intel	Do not use
14	Reserved by Intel	Do not use
15	Reserved by Intel	Do not use
16	Reserved by Intel	Do not use
17	GND	System Ground
18	Vcc	Sensors Reference Voltage



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Title

DEBUG (LPC DEBUG)

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SENSOR (RSVD)			
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# Angle Calculation (ISH\_I2C)

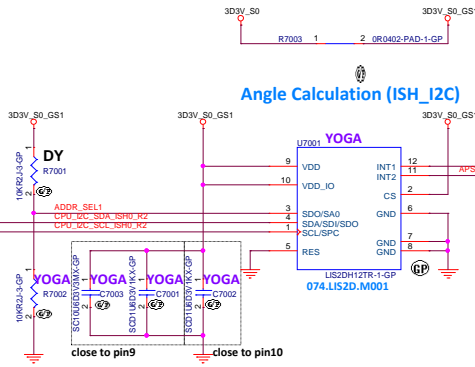


TABLE for Angle Detection (U7001): Tri-axis Digital Accelerometer

P/N	ADDR_SEL1	Address (7bit)
ST LIS2DH12TR	H	19h (7bit)
	L	18h (7bit)

(SENSOR BD)  
LOGIC (MB)

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

LOGIC

TABLE of G-Sensor (U7001)

Vendor	P/N	Wistron P/N
ST	LIS2DH12TR	074.LIS2D.M001

# Thermal Control (I2C)

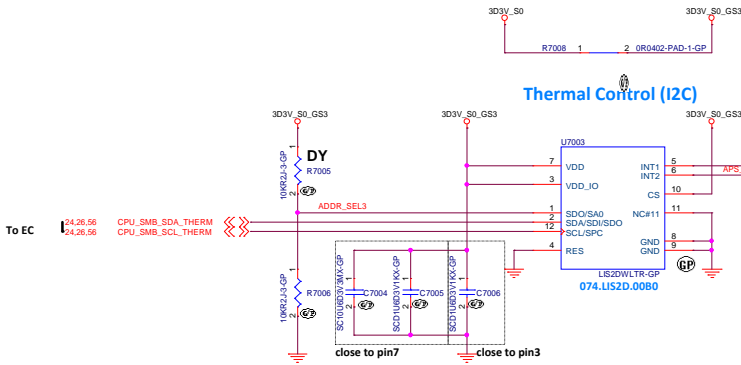


TABLE for ITS Detection (U7003): Tri-axis Digital Accelerometer

P/N	ADDR_SEL3	Address (8bit)
ST LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

LOGIC

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode

LOGIC

TABLE of G-Sensor (U7003)

Vendor	P/N	Wistron P/N
ST	LIS2DWLR	074.LIS2D.0080

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File	Document Number	Rev
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TitleEXT IO (RSVD)	
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TitleEXT IO (RSVD)	
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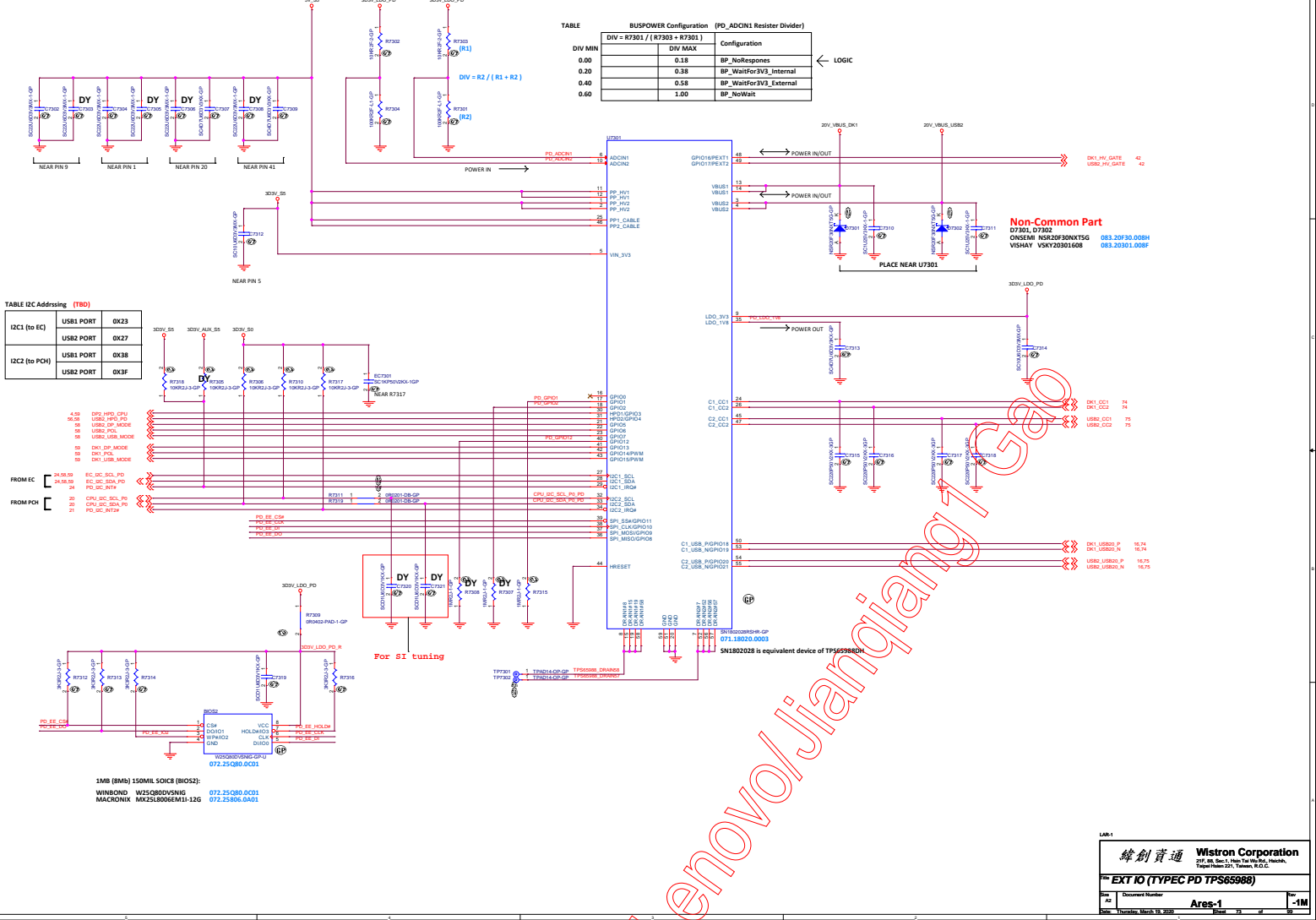


TABLE BUSPOWER Configuration (PD\_ADCIN1 Resistor Divider)

DIV MIN	DIV MAX	Configuration
0.00	0.18	BP_NoResponses
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

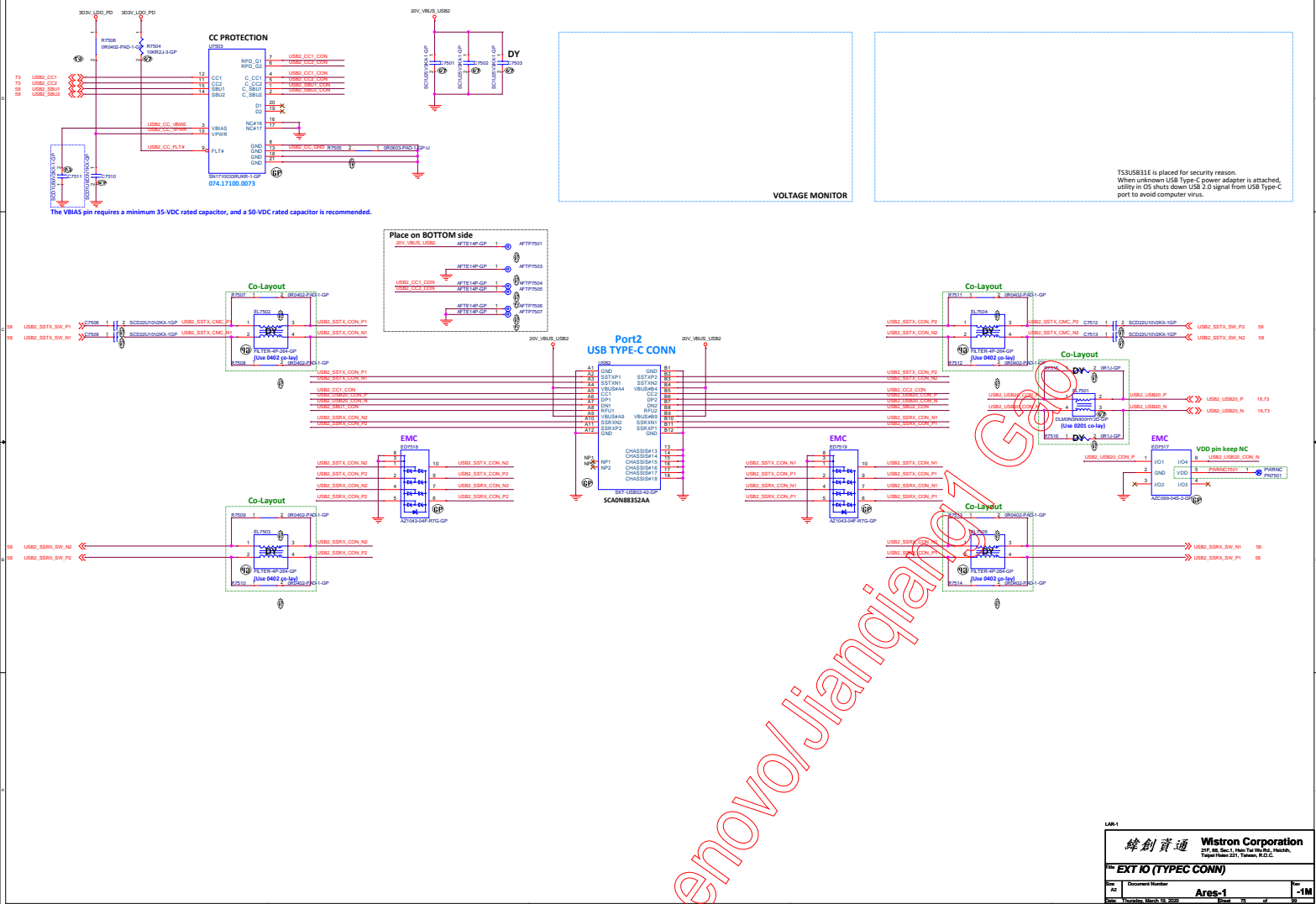
TABLE I2C Addressing (TBD)

I2C1 (to EC)	USB1 PORT	0X23
	USB2 PORT	0X27
I2C2 (to PCH)	USB1 PORT	0X38
	USB2 PORT	0X3F

Non-Common Part  
D7301, D7302  
ONSEMI NOK20F30NXTSG 083.20F30.008H  
VISHAY VSKY20301608 083.20301.008F

Wistron Corporation  
EXT IO (TYPEC PD TPS65988)  
Ares-1  
Date: November 18, 2020





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GPU (RSVD)			
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Title			
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TitleGPU (RSVD)		
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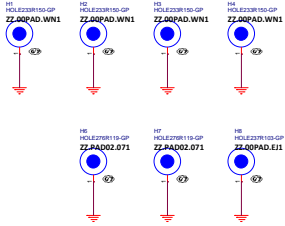
LAR-1		
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TitleGPU (RSVD)		
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EMI Spring

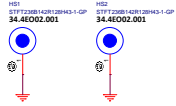


Screw Pad

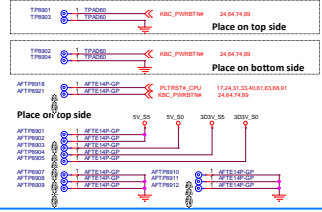


RF CAPS

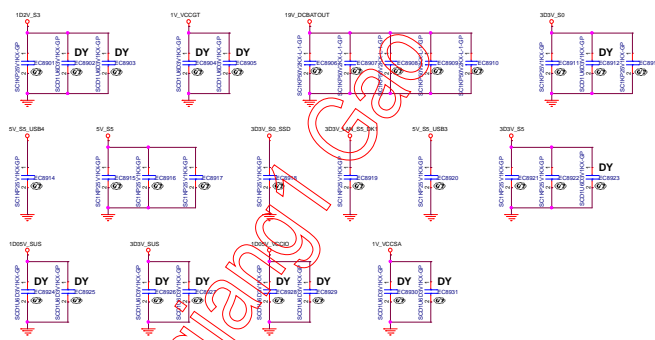
Stand Off



Test Point



EMI CAPS



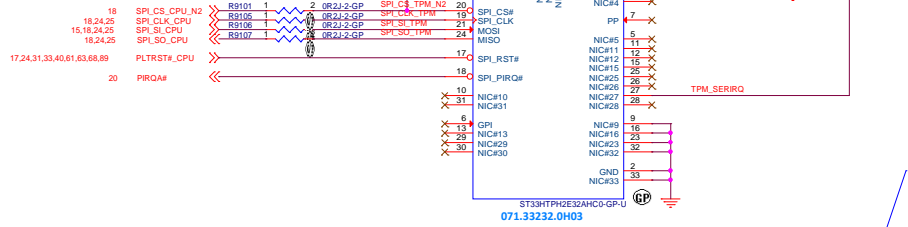
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TitleINT IO (RSVD)		
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For SPI Chip Select Function:  
External 10K-ohm pull-up (R9103)

ST: Optional  
NuvoTon: MUST



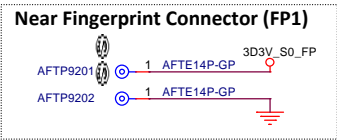
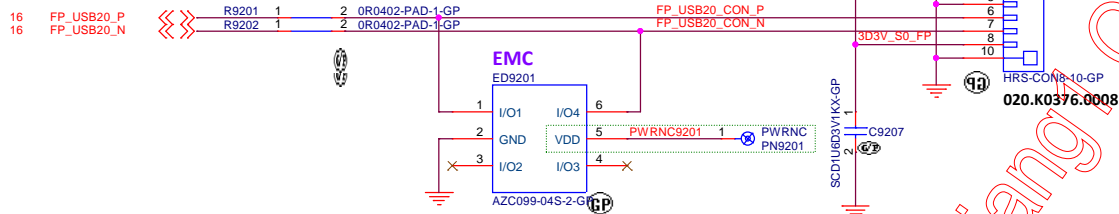
SPI Chip Select Pin:  
ST (SPI\_CS#) Internal pull-up  
NuvoTon (SCS#) Internal pull-up is disabled if the pin is part of the recognized host interface

TABLE		
1st	ST33HTPH2E32AHCO	071.33232.0H03
2nd	NPCT750LABYX	071.00750.0D03

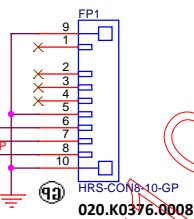
TABLE				
		071.33232.0H03	071.00750.0D03	071.00750.0D03
Pin No	TCG PTP Spec(V38)	ST Micro ST33HTPH2E32AHCO	NuvoTon NPCT750LABYX	Indefinite
1	VDD	NC	VSB	VDD
2	GND	NC	NC	GND
3	NC	NC	NC	NC
4	GPIO	NC	GPIO/PP	GPIO
5	NC	NC	NC	NC
6	GPIO	NC	GPIO3	GPIO
7	GPIO	NC	NC	GPIO
8	VDD	NC	VHIO	VDD
9	NC	NC	NC	NC
10	NC	NC	NC	NC
11	NC	NC	NC	NC
12	NC	NC	NC	NC
13	GPIO	NC	GPIO4	GPIO
14	NC	NC	NC	NC
15	NC	NC	NC	NC
16	GND	NC	GND	GND
17	SPI_RST#	SPI_RST#	RST#	RST#
18	SPI_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	PIRQ#
19	SPI_CLK	SPI_CLK	SCLK	SCLK
20	SPI_CSH	SPI_CSH	SCS#/GPIO5	SCS#
21	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VPS	VHIO	VDD
23	GND	NC	GND	GND
24	MISO	NC	MISO	MISO
25	NC	NC	NC	NC
26	NC	NC	NC	NC
27	NC	NC	NC	NC
28	NC	NC	NC	NC
29	SDA/GPIO1	NC	SDA/GPIO0	SDA
30	SDA/GPIO0	NC	SCL/GPIO1	SCL
31	NC	NC	NC	NC
32	NC	NC	NC	NC

LAR-1

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File INT IO (TPM 2.0)			
Size A3	Document Number	Ares-1	
Date: Thursday, March 16, 2020		Sheet 91	Rev -1M

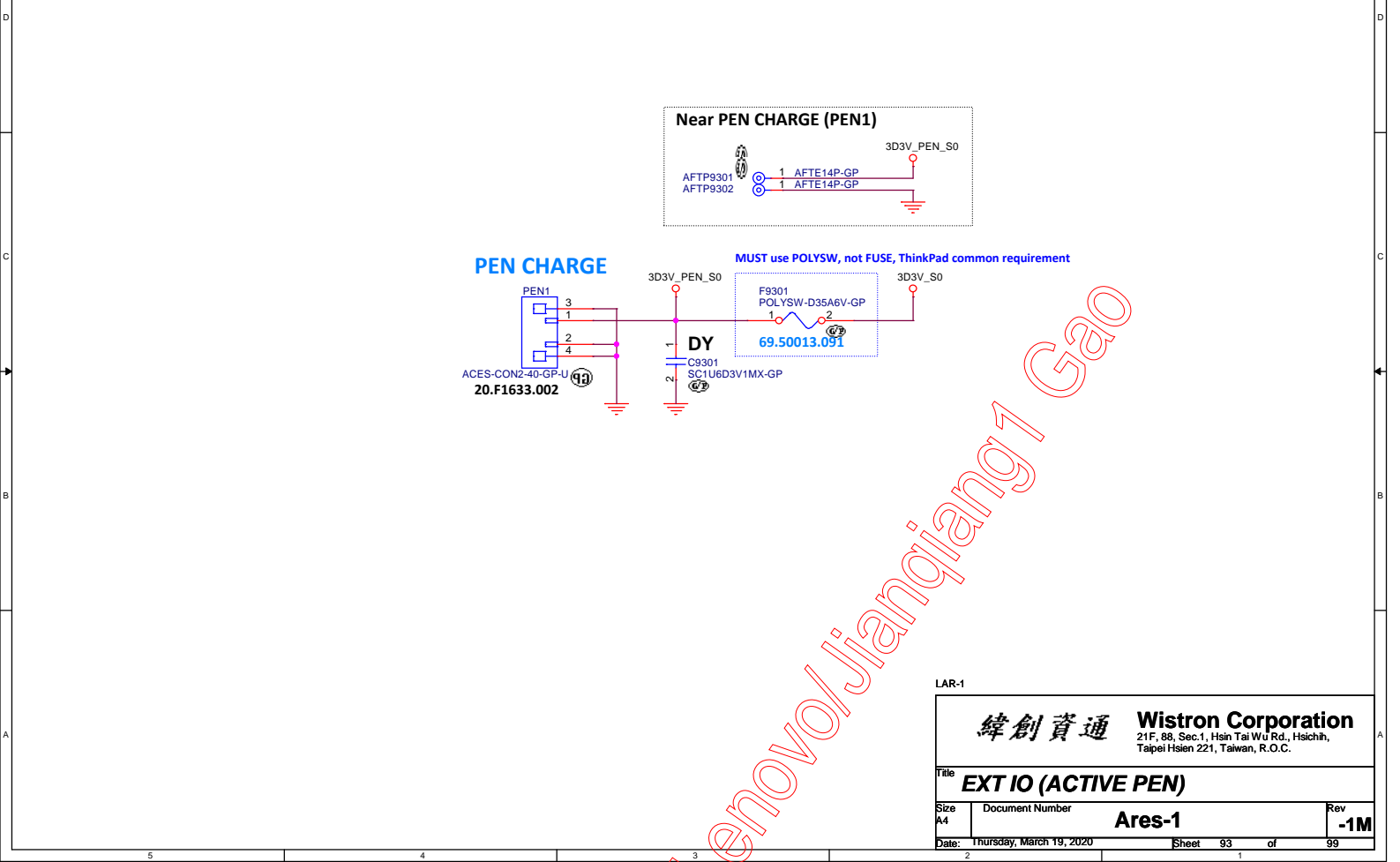


### Fingerprint Connector



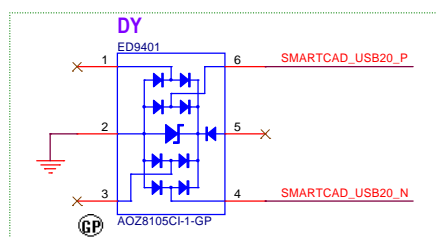
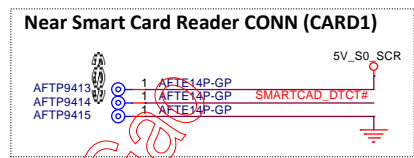
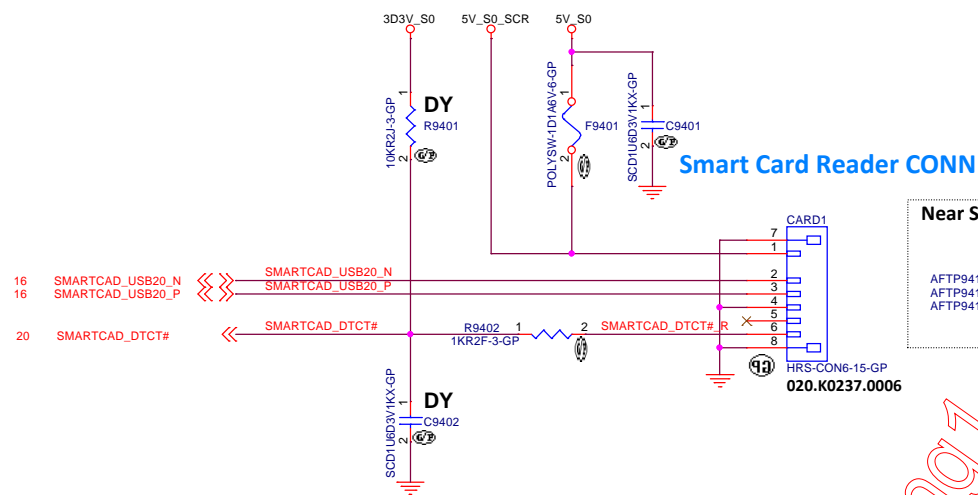
LAR-1

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title INT IO (FINGERPRINT)</b>	
Size A4	Document Number <b>Ares-1</b>
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Title			
<b>EXT IO (ACTIVE PEN)</b>			
Size	Document Number		Rev
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2			1



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Title			
EXT IO (SMART CARD)			
Size	Document Number	Rev	
A4	Ares-1	-1M	
Date:	Thursday, March 19, 2020	Sheet	94 of 99

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Title			
EXT IO (RSVD)			
Size	Document Number		Rev
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<div>緯創資通Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title COMMERCIAL (RSVD)		
Size A4	Document Number Ares-1	Rev -1M
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Title			
COMMERCIAL (RSVD)			
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Title			
COMMERCIAL (RSVD)			
Size	Document Number		Rev
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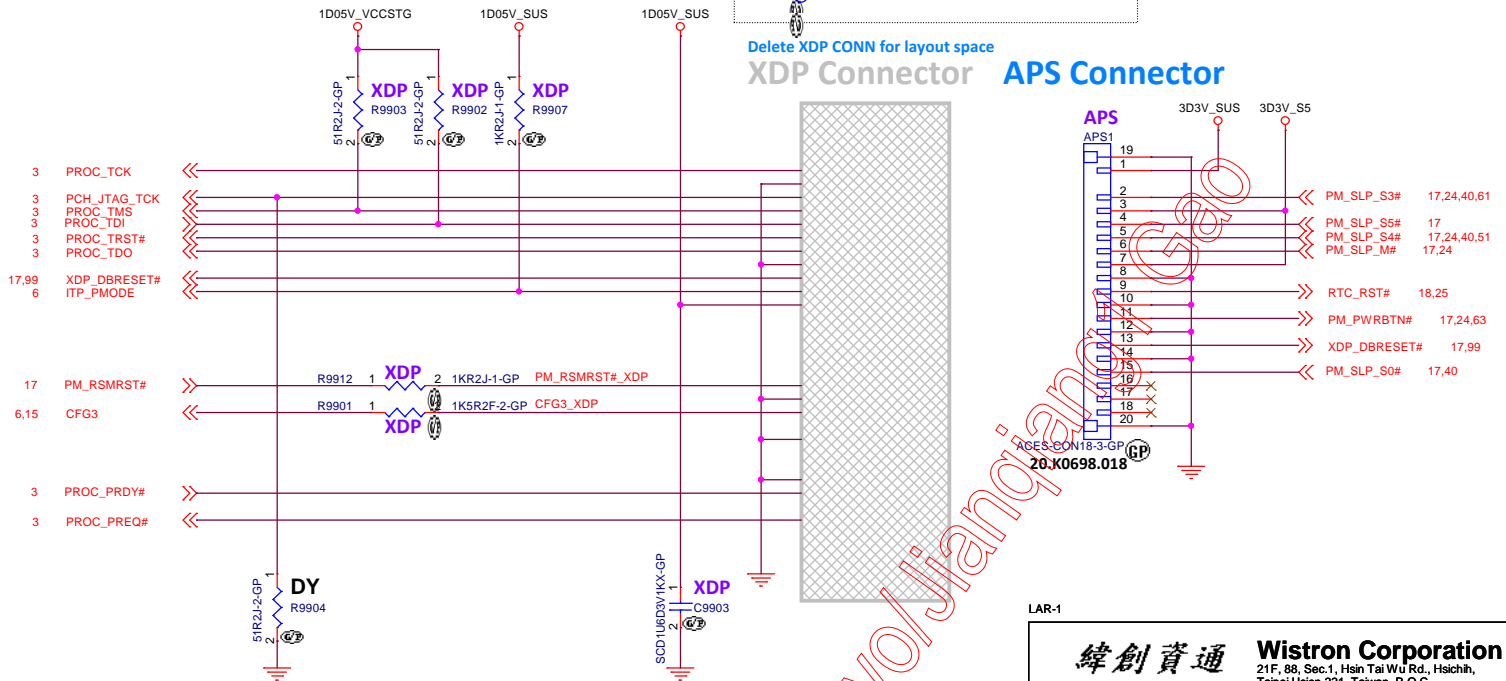
## XDP Test Point

TP9901	1	TPAD14-OP-GP	PROC_TCK
TP9902	1	TPAD14-OP-GP	PCH_JTAG_TCK
TP9903	1	TPAD14-OP-GP	PROC_TMS
TP9904	1	TPAD14-OP-GP	PROC_TDI
TP9905	1	TPAD14-OP-GP	PROC_TRST#
TP9906	1	TPAD14-OP-GP	PROC_TDO
TP9907	1	TPAD14-OP-GP	XDP_DBRESET#
TP9908	1	TPAD14-OP-GP	ITP_PMODE
TP9909	1	TPAD14-OP-GP	1D05V_SUS
TP9910	1	TPAD14-OP-GP	PM_RSMRST#_XDP
TP9911	1	TPAD14-OP-GP	CFG3_XDP
TP9912	1	TPAD14-OP-GP	PROC_PRDY#
TP9913	1	TPAD14-OP-GP	PROC_PREQ#

Delete XDP CONN for layout space

XDP Connector

APS Connector



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**DEBUG (XDP/APS)**

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